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EVALUATION KIT AVAILABLE

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller



## General Description

The MAX8796/MAX8797/MAX17401 are 1-phase Quick-PWM™ step-down VID power-supply controllers for Intel notebook CPUs and graphics. The Quick-PWM control provides instantaneous response to fast load current steps. Active voltage positioning reduces power dissipation and bulk output capacitance requirements and allows ideal positioning compensation for tantalum, polymer, or ceramic bulk output capacitors.

The MAX8796/MAX8797/MAX17401 are intended for two different notebook CPU/GPU core applications: either bucking down the battery directly to create the core voltage, or else bucking down the +5V system supply. The single-stage conversion method allows this device to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, 2-stage conversion (stepping down the +5V system supply instead of the battery) at higher switching frequency provides the minimum possible physical size.

A slew-rate controller allows controlled transitions between VID codes. A thermistor-based temperature sensor provides programmable thermal protection. A power monitor provides an analog voltage output proportional to the power consumed by the CPU/GPU.

The MAX8796/MAX17401 implement both the Intel IMVP-6 CPU core specifications, as well as the Intel GMCH graphics core specifications. The MAX8797 implements the Intel GMCH graphics core specifications. The MAX8796/MAX17401 are available in a 32-pin TQFN package. The MAX8797 is available in a 28-pin TQFN package.

## Applications

IMVP-6/IMVP-6+ Core Power Supply
Intel GMCH Crestline/Cantiga

Graphics Core Power Supply

Voltage-Positioned Step-Down Converters

2 to 4 Lithium-Ion (Li+) Cell Battery-to-CPU Core Supply Converters

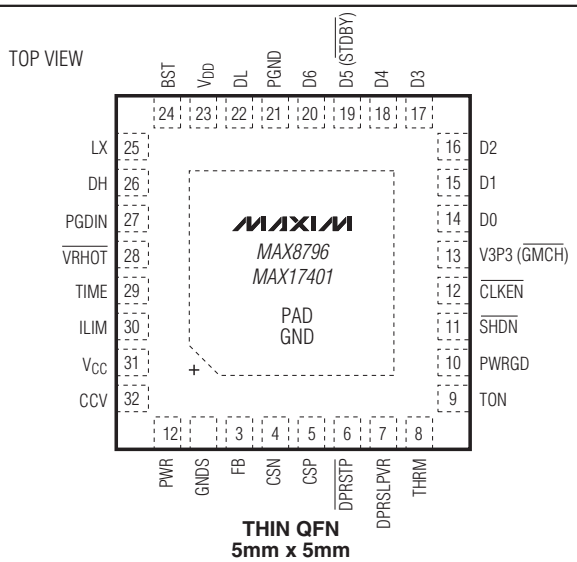
Notebooks/Desktops/Servers

*Quick-PWM is a trademark of Maxim Integrated Products, Inc.*

## Features

- **1-Phase Quick-PWM Controller**
- **±0.5% $V_{OUT}$ Accuracy Over Line, Load, and Temperature**
- **7-Bit IMVP-6 DAC (MAX8796/MAX17401 Only)**
- **5-Bit GMCH DAC**
- **Active Voltage Positioning with Adjustable Gain**
- **Accurate Droop and Current Limit**
- **Remote Output and Ground Sense**
- **Adjustable Output-Voltage Slew Rate**
- **Power-Good Window Comparator**
- **Power Monitor**
- **Temperature Comparator**
- **Drives Large Synchronous Rectifier FETs**
- **2V to 26V Power Input Range**
- **Adjustable Switching Frequency (600kHz max)**
- **Output Overvoltage Protection (MAX8796/MAX8797 Only)**
- **Undervoltage and Thermal-Fault Protection**
- **Soft-Startup and Soft-Shutdown**
- **Internal Boost Diodes**

## Pin Configurations




**THIN QFN**
**5mm x 5mm**

*Pin Configurations continued at end of data sheet.*

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | FEATURE |
|---|---|---|---|
| **MAX8796**GTJ+ | -40°C to +105°C | 32 TQFN | IMVP-6/GMCH |
| **MAX8797**GTI+ | -40°C to +105°C | 28 TQFN | GMCH only |
| **MAX17401**GTJ+ | -40°C to +105°C | 32 TQFN | IMVP-6/GMCH |

*+Denotes a lead-free/RoHS-compliant package.*

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$, $V_{DD}$ to GND .....-0.3V to +6V
CSP, CSN to GND .....-0.3V to +6V
ILIM, THRM, DPRSLPVR, $\overline{VRHOT}$, PWRGD to GND .....-0.3V to +6V
CCV, FB, PWR, TIME to GND .....-0.3V to ($V_{CC}$ + 0.3V)
$\overline{SHDN}$ to GND (Note 1) .....-0.3V to +30V
TON to GND .....-0.3V to +30V
GNDS, PGND to GND .....-0.3V to +0.3V
DL to PGND .....-0.3V to ($V_{DD}$ + 0.3V)
BST to GND .....-0.3V to +36V
LX to BST .....-6V to +0.3V
BST to $V_{DD}$ .....-0.3V to +30V
DH to LX .....-0.3V to ($V_{BST}$ + 0.3V)
**MAX8796/MAX17401 Only:**
V3P3 to GND .....-0.3V to +6V
$\overline{CLKEN}$ to GND .....-0.3V to (V3P3 + 0.3V)
D0–D6 to GND .....-0.3V to +6V
PGDIN, $\overline{DPRSTP}$ to GND .....-0.3V to +6V
**MAX8797 Only:**
D0–D4, $\overline{STDBY}$ to GND .....-0.3V to +6V
MAX8796/MAX17401 32-Pin, 5mm x 5mm TQFN Continuous Power Dissipation (up to +70°C) (derate above +70°C/21.3mW/°C) .....1702mW
MAX8797 28-Pin, 4mm x 4mm TQFN Continuous Power Dissipation (up to +70°C) (derate above +70°C/20.8mW/°C) .....1667mW
Operating Temperature Range .....-40°C to +105°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

**Note 1:** $\overline{SHDN}$ can be forced to 12V for the purpose of debugging prototype breadboards using the no-fault test mode, which disables fault protection.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1 (MAX8796/MAX17401), Circuit of Figure 2 (MAX8797), $V_{IN}$ = 12V, $V_{DD}$ = $V_{CC}$ = 5V, V3P3 = 3.3V, $\overline{SHDN}$ = $\overline{STDBY}$ = $\overline{DPRSTP}$ = ILIM = PGDIN = $V_{CC}$, DPRSLPVR = GNDS = PGND = GND, $R_{FB}$ = 4.25kΩ, $V_{CC\_SENSE}$ = $V_{CSP}$ = $V_{CSN}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100 for IMVP-6, D0–D4 = 01000 for GMCH). **$T_A$ = 0°C to +85°C**, unless otherwise specified. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **PWM CONTROLLER** | | | | | | | |
| Input Voltage Range | | $V_{CC}$, $V_{DD}$ | | 4.5 | | 5.5 | V |
| | | V3P3 (MAX8796/MAX17401 only) | | 3.0 | | 3.6 | |
| DC Output-Voltage Accuracy | | Measured at FB with respect to GNDS; includes load-regulation error (Note 3) | DAC codes from 0.8125V to 1.5000V | -0.5 | | +0.5 | % |
| | | | DAC codes from 0.3750V to 0.8000V | -7 | | +7 | mV |
| | | | DAC codes from 0 to 0.3625V | -20 | | +20 | |
| IMVP-6 Boot Voltage | $V_{BOOT}$ | IMVP-6 (MAX8796/MAX17401 only) | | 1.194 | 1.200 | 1.206 | V |
| Line Regulation Error | | $V_{CC}$ = 4.5V to 5.5V, $V_{IN}$ = 4.5V to 26V | | | 0.1 | | % |
| GNDS Input Range | | | | -200 | | +200 | mV |
| GNDS Gain | $A_{GNDS}$ | $\Delta V_{OUT}/\Delta V_{GNDS}$, -200mV ≤ $V_{GNDS}$ ≤ +200mV | | 0.97 | 1.00 | 1.03 | V/V |
| GNDS Input Bias Current | $I_{GNDS}$ | | | -15 | -10 | +2 | µA |
| TIME Voltage | $V_{TIME}$ | $V_{CC}$ = 4.5V to 5.5V, $I_{TIME}$ = 28µA ($R_{TIME}$ = 71.5kΩ) | | 1.985 | 2.000 | 2.015 | V |

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1 (MAX8796/MAX17401), Circuit of Figure 2 (MAX8797), $V_{IN}$ = 12V, $V_{DD}$ = $V_{CC}$ = 5V, V3P3 = 3.3V, $\overline{SHDN}$ = $\overline{STDBY}$ = $\overline{DPRSTP}$ = ILIM = PGDIN = $V_{CC}$, DPRSLPVR = GNDS = PGND = GND, $R_{FB}$ = 4.25kΩ, $V_{CC\_SENSE}$ = $V_{CSP}$ = $V_{CSN}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100 for IMVP-6, D0–D4 = 01000 for GMCH). **$T_A$ = 0°C to +85°C**, unless otherwise specified. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| TIME Slew-Rate Accuracy | | $R_{TIME}$ = 71.5kΩ (12.5mV/µs nominal) | | -10 | | +10 | % |
| | | $R_{TIME}$ = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal) | | -15 | | +15 | |
| | | Soft-start and soft-shutdown; $R_{TIME}$ = 35.7kΩ (3.125mV/µs nominal) to 178kΩ (0.625mV/µs nominal) | | -20 | | +20 | |
| | | IMVP-6 slow C4 exit (MAX8796/MAX17401 only)—$\overline{DPRSTP}$ = DPRSLPVR = $V_{CC}$; $R_{TIME}$ = 35.7kΩ (6.25mV/µs nominal) to 178kΩ (1.25mV/µs nominal) | | -20 | | +20 | |
| On-Time (Note 4) | $t_{ON}$ | $V_{IN}$ = 12V | $R_{TON}$ = 96.75kΩ | 142 | 167 | 192 | ns |
| | | $V_{FB}$ = 1.2V | $R_{TON}$ = 200kΩ | 300 | 333 | 366 | |
| | | | $R_{TON}$ = 303.25kΩ | 425 | 500 | 575 | |
| Minimum Off-Time | $t_{OFF(MIN)}$ | Measured at DH (Note 4) | | | 300 | 375 | ns |
| TON Shutdown Input Current | | $\overline{SHDN}$ = GND, $V_{IN}$ = 26V, $V_{CC}$ = $V_{DD}$ = 0V or 5V, $T_A$ = +25°C | | | 0.01 | 1 | µA |
| **BIAS CURRENTS** | | | | | | | |
| Quiescent Supply Current ($V_{CC}$) | $I_{CC}$ | Measured at $V_{CC}$, DPRSLPVR = 5V, FB forced above the regulation point | | | 1.5 | 4 | mA |
| Quiescent Supply Current ($V_{DD}$) | $I_{DD}$ | Measured at $V_{DD}$, DPRSLPVR = 0V, FB forced above the regulation point, $T_A$ = +25°C | | | 0.02 | 1 | µA |
| Quiescent Supply Current (V3P3) (MAX8796/MAX17401 Only) | $I_{3P3}$ | Measured at V3P3, FB forced within the $\overline{CLKEN}$ power-good window | | | 2 | 4 | µA |
| Shutdown Supply Current ($V_{CC}$) | | Measured at $V_{CC}$, $\overline{SHDN}$ = GND, $T_A$ = +25°C | | 0.01 | | 1 | µA |
| Shutdown Supply Current ($V_{DD}$) | | Measured at $V_{DD}$, $\overline{SHDN}$ = GND, $T_A$ = +25°C | | 0.01 | | 1 | µA |
| Shutdown Supply Current (V3P3) (MAX8796/MAX17401 Only) | | Measured at V3P3, $\overline{SHDN}$ = GND, $T_A$ = +25°C | | | 0.01 | 1 | µA |
| **FAULT PROTECTION** | | | | | | | |
| Output Overvoltage-Protection Threshold (MAX8796/MAX8797 Only) | $V_{OVP}$ | Skip mode after output reaches the regulation voltage or PWM mode; measured at FB with respect to typical VID target specified in Table 3 (IMVP-6) and Table 4 (GMCH) | | 250 | 300 | 350 | mV |
| | | Soft-start, soft-shutdown, skip mode, and output have not reached the regulation voltage; measured at FB | IMVP-6 (MAX8796 only) | 1.75 | 1.80 | 1.85 | V |
| | | | GMCH (MAX8796 with V3P3 = GND and MAX8797) | 1.50 | 1.55 | 1.60 | |
| | | Minimum OVP threshold; measured at FB | | | 0.8 | | |

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller



## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1 (MAX8796/MAX17401), Circuit of Figure 2 (MAX8797), $V_{IN}$ = 12V, $V_{DD}$ = $V_{CC}$ = 5V, V3P3 = 3.3V, $\overline{SHDN}$ = $\overline{STDBY}$ = $\overline{DPRSTP}$ = ILIM = PGDIN = $V_{CC}$, DPRSLPVR = GNDS = PGND = GND, $R_{FB}$ = 4.25kΩ, $V_{CC\_SENSE}$ = $V_{CSP}$ = $V_{CSN}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100 for IMVP-6, D0–D4 = 01000 for GMCH). **$T_A$ = 0°C to +85°C**, unless otherwise specified. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output Overvoltage Propagation Delay (MAX8796/MAX8797 Only) | $t_{OVP}$ | FB forced 25mV above trip threshold | | | 10 | | µs |
| Output Undervoltage-Protection Threshold | $V_{UVP}$ | Measured at FB with respect to typical VID target specified in Table 3 (IMVP-6) and Table 4 (GMCH) | | -450 | -400 | -350 | mV |
| Output Undervoltage Propagation Delay | $t_{UVP}$ | FB forced 25mV below trip threshold | | | 10 | | µs |
| IMVP-6 $\overline{CLKEN}$ Startup Delay (Boot Time Period, MAX8796/MAX17401 Only) | $t_{BOOT}$ | IMVP-6: MAX8796/MAX17401 V3P3 = 3.3V; measured from the time when FB reaches the boot target voltage (Note 3); the time needed for FB to reach this target voltage is based on the slew rate set by $R_{TIME}$ | | 20 | 60 | 100 | µs |
| PWRGD Startup Delay | | IMVP-6: MAX8796/MAX17401 V3P3 = 3.3V; measured at startup from the time when $\overline{CLKEN}$ goes low | | 3 | 5 | 8 | ms |
| | | GMCH: MAX8797 or MAX8796/MAX17401 V3P3 = GND; measured from the time when FB reaches the target voltage (Note 3); the time needed for FB to reach this target voltage is based on the slew rate set by $R_{TIME}$ | | 20 | 60 | 100 | µs |
| PWRGD Standby Wake-Up Delay | | GMCH: MAX8797 or MAX8796/MAX17401 V3P3 = GND; measured from the time when FB reaches the target voltage (Note 3) based on the slew rate set by $R_{TIME}$ | | | 20 | | µs |
| PWRGD and $\overline{CLKEN}$ (MAX8796/MAX17401 IMVP-6 Only) Threshold | | Measured at FB with respect to typical VID target specified in Table 3 (IMVP-6) and Table 4 (GMCH); 50mV hysteresis (typ) | Lower threshold, falling edge (undervoltage) | -350 | -300 | -250 | mV |
| | | | Upper threshold, rising edge (overvoltage) | +150 | +200 | +250 | |
| PWRGD and $\overline{CLKEN}$ (MAX8796/MAX17401 IMVP-6 Only) Transition Blanking Time | $t_{BLANK}$ | Measured from the time when FB reaches the target voltage (Note 3) based on the slew rate set by $R_{TIME}$ | | | 20 | | µs |
| PWRGD and $\overline{CLKEN}$ (MAX8796/MAX17401 Only) Delay | | FB forced 25mV outside the PWRGD trip thresholds | | | 10 | | µs |
| IMVP-6 $\overline{CLKEN}$ Output Low Voltage (MAX8796/MAX17401 Only) | | IMVP-6: MAX8796/MAX17401, V3P3 = 3.3V; $I_{SINK}$ = 3mA | | | | 0.4 | V |
| IMVP-6 $\overline{CLKEN}$ Output High Voltage (MAX8796/MAX17401 Only) | | IMVP-6: MAX8796/MAX17401 V3P3 = 3.3V; $I_{SOURCE}$ = 3mA | | V3P3 - 0.4 | | | V |
| PWRGD Output Low Voltage | | $I_{SINK}$ = 3mA | | | | 0.4 | V |
| PWRGD Leakage Current | | High state, PWRGD forced to 5V, $T_A$ = +25°C | | | | 1 | µA |

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1 (MAX8796/MAX17401), Circuit of Figure 2 (MAX8797), $V_{IN}$ = 12V, $V_{DD}$ = $V_{CC}$ = 5V, V3P3 = 3.3V, $\overline{SHDN}$ = $\overline{STDBY}$ = $\overline{DPRSTP}$ = ILIM = PGDIN = $V_{CC}$, DPRSLPVR = GNDS = PGND = GND, $R_{FB}$ = 4.25kΩ, $V_{CC\_SENSE}$ = $V_{CSP}$ = $V_{CSN}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100 for IMVP-6, D0–D4 = 01000 for GMCH). **$T_A$ = 0°C to +85°C**, unless otherwise specified. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ Undervoltage Lockout Threshold | $V_{UVLO(VCC)}$ | Rising edge, 65mV typical hysteresis, controller disabled below this level | | 4.05 | 4.27 | 4.48 | V |
| CSN Discharge Resistance in UVLO and Shutdown | | $\overline{SHDN}$ = GND; measured when soft-shutdown has been completed (DL pulled low) | | | 8 | | Ω |
| **THERMAL COMPARATOR AND PROTECTION** | | | | | | | |
| $\overline{VRHOT}$ Trip Threshold | | Measured at THRM with respect to $V_{CC}$; falling edge; typical hysteresis = 100mV | | 29.2 | 30 | 30.8 | % |
| $\overline{VRHOT}$ Delay | $t_{\overline{VRHOT}}$ | THRM forced 25mV below the $\overline{VRHOT}$ trip threshold; falling edge | | | 10 | | µs |
| $\overline{VRHOT}$ Output On-Resistance | $R_{\overline{VRHOT}}$ | Low state | | | 2 | 8 | Ω |
| $\overline{VRHOT}$ Leakage Current | $I_{\overline{VRHOT}}$ | High state, $\overline{VRHOT}$ forced to 5V, $T_A$ = +25°C 1 | | | | | µA |
| THRM Input Leakage | $I_{THRM}$ | $V_{THRM}$ = 0 to 5V, $T_A$ = +25°C | | -100 | | +100 | nA |
| Thermal-Shutdown Threshold | $T_{SHDN}$ | Typical hysteresis = 15°C | | | 160 | | °C |
| **VALLEY CURRENT LIMIT AND DROOP** | | | | | | | |
| Current-Limit Threshold Voltage (Positive Adjustable) | $V_{LIMIT}$ | $V_{CSP}$ - $V_{CSN}$ | $V_{TIME}$ - $V_{ILIM}$ = 100mV | 7 | 10 | 13 | mV |
| | | | $V_{TIME}$ - $V_{ILIM}$ = 500mV | 45 | 50 | 55 | |
| Current-Limit Threshold Voltage (Positive Default) | | $V_{CSP}$ - $V_{CSN}$ | IMVP-6 (MAX8796/ MAX17401 only) | 20 | 22.5 | 25 | mV |
| | | ILIM = $V_{CC}$ | GMCH (MAX8796/ MAX17401 V3P3 = GND or MAX8797) | 15 | 17.5 | 20 | |
| Current-Limit Threshold Voltage (Negative) Accuracy | $V_{LIMIT(NEG)}$ | $V_{CSP}$ - $V_{CSN}$, nominally -125% of $V_{LIMIT}$ | | -4 | | +4 | mV |
| Current-Limit Threshold Voltage (Zero Crossing) | $V_{ZERO}$ | $V_{PGND}$ - $V_{LX}$, DPRSLPVR = $V_{CC}$ | | | 1 | | mV |
| CSP, CSN Common-Mode Input Range | | | | 0 | | 2 | V |
| CSP, CSN Input Current | | $T_A$ = +25°C | | -0.2 | | +0.2 | µA |
| ILIM Input Current | | $T_A$ = +25°C | | -100 | | +100 | nA |
| Droop Amplifier (GMD) Offset | | ($V_{CSP}$ - $V_{CSN}$) at $I_{FB}$ = 0 | | -0.75 | | +0.75 | mV |
| Droop Amplifier (GMD) Transconductance | | $\Delta I_{FB}/\Delta(V_{CSP} - V_{CSN})$; FB = CSN = 0.45V to 2.0V, and ($V_{CSP}$ - $V_{CSN}$) = -15.0mV to +15.0mV | | 592 | 600 | 608 | µS |
| **POWER MONITOR (PWR)** | | | | | | | |
| Power Monitor Output Voltage for Typical HFM Conditions | $V_{PWR}$ | $V_{CSN}$ - $V_{GNDS}$ = 1.200V | $V_{TIME}$ - $V_{ILIM}$ = 225mV, $V_{CSP}$ - $V_{CSN}$ = 15mV | 1.95 | 2.00 | 2.05 | V |
| | | $I_{PWR}$ = 0µA | $V_{TIME}$ - $V_{ILIM}$ = 500mV, $V_{CSP}$ - $V_{CSN}$ = 15mV | 0.868 | 0.90 | 0.932 | |
| Power Monitor Gain Referred to Output Voltage ($V_{CSN}$ - $V_{GNDS}$) | $A_{VPWR}$ | $V_{TIME}$ - $V_{ILIM}$ = 225mV, $V_{CSP}$ - $V_{CSN}$ = 15mV | | 1.625 | 1.67 | 1.708 | V/V |

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## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1 (MAX8796/MAX17401), Circuit of Figure 2 (MAX8797), $V_{IN}$ = 12V, $V_{DD}$ = $V_{CC}$ = 5V, V3P3 = 3.3V, $\overline{SHDN}$ = $\overline{STDBY}$ = $\overline{DPRSTP}$ = ILIM = PGDIN = $V_{CC}$, DPRSLPVR = GNDS = PGND = GND, $R_{FB}$ = 4.25kΩ, $V_{CC\_SENSE}$ = $V_{CSP}$ = $V_{CSN}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100 for IMVP-6, D0–D4 = 01000 for GMCH). **$T_A$ = 0°C to +85°C**, unless otherwise specified. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Power Monitor Gain Referred to Current Sense ($V_{CSP}$ - $V_{CSN}$) | $A_{IPWR}$ | $V_{TIME}$ - $V_{ILIM}$ = 225mV, $V_{CSN}$ - $V_{GNDS}$ = 1.200V | | 122 | 133 | 144 | V/V |
| Power Monitor Load Regulation | $\Delta V_{PWR}$ | Measured at PWR with respect to unloaded voltage | Source: $I_{PWR}$ = 0µA to 500µA | -3 | | | mV |
| | | | Sink: $I_{PWR}$ = -100µA | | 50 | | |
| **GATE DRIVERS** | | | | | | | |
| DH Gate-Driver On-Resistance | $R_{ON(DH)}$ | BST - LX forced to 5V | High state (pullup) | | 0.9 | 2.5 | Ω |
| | | | Low state (pulldown) | | 0.7 | 2.0 | |
| DL Gate-Driver On-Resistance | $R_{ON(DL)}$ | | High state (pullup) | | 0.7 | 2.0 | Ω |
| | | | Low state (pulldown) | | 0.25 | 0.7 | |
| DH Gate-Driver Source Current | $I_{DH(SOURCE)}$ | DH forced to 2.5V, BST - LX forced to 5V | | | 2.2 | | A |
| DH Gate-Driver Sink Current | $I_{DH(SINK)}$ | DH forced to 2.5V, BST - LX forced to 5V | | | 2.7 | | A |
| DL Gate-Driver Source Current | $I_{DL(SOURCE)}$ | DL forced to 2.5V | | | 2.7 | | A |
| DL Gate-Driver Sink Current | $I_{DL(SINK)}$ | DL forced to 2.5V | | | 8 | | A |
| Driver Propagation Delay (Driver Dead Time) | | DH low to DL high | | | 20 | | ns |
| | | DL low to DH high | | | 20 | | |
| DL Transition Time | | DL falling, $C_{DL}$ = 3nF | | | 20 | | ns |
| | | DL rising, $C_{DL}$ = 3nF | | | 20 | | |
| DH Transition Time | | DH falling, $C_{DH}$ = 3nF | | | 20 | | ns |
| | | DH rising, $C_{DH}$ = 3nF | | | 20 | | |
| Internal BST Switch On-Resistance | $R_{BST}$ | $I_{BST}$ = 10mA, $V_{DD}$ = 5V | | | 10 | 20 | Ω |
| **LOGIC AND I/O** | | | | | | | |
| Logic Input High Voltage | $V_{IH}$ | MAX8796/MAX17401: $\overline{SHDN}$, DPRSLPVR, PGDIN; MAX8797: $\overline{SHDN}$, DPRSLPVR; rising edge, typical hysteresis = 250mV | | 2.3 | | | V |
| Logic Input Low Voltage | $V_{IL}$ | MAX8796/MAX17401: $\overline{SHDN}$, DPRSLPVR, PGDIN; MAX8797: $\overline{SHDN}$, DPRSLPVR; falling edge, typical hysteresis = 250mV | | | | 1.0 | V |
| Low-Voltage Logic Input High Voltage | $V_{IHLV}$ | MAX8796/MAX17401: $\overline{DPRSTP}$, D0–D6; MAX8797: $\overline{STDBY}$, D0–D4; rising edge, typical hysteresis = 90mV | | 0.67 | | | V |
| Low-Voltage Logic Input Low Voltage | $V_{ILLV}$ | MAX8796/MAX17401: $\overline{DPRSTP}$, D0–D6; MAX8797: $\overline{STDBY}$, D0–D4; falling edge, typical hysteresis = 90mV | | | | 0.33 | V |
| Logic Input Current | | $T_A$ = +25°C; MAX8796/MAX17401: $\overline{SHDN}$, DPRSLPVR, PGDIN, $\overline{DPRSTP}$, D0–D6 = 0 or 5V; MAX8797: $\overline{SHDN}$, DPRSLPVR, $\overline{STDBY}$, D0–D4 = 0 or 5V | | -1 | | +1 | µA |

## ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1 (MAX8796/MAX17401), Circuit of Figure 2 (MAX8797), $V_{IN}$ = 12V, $V_{DD}$ = $V_{CC}$ = 5V, V3P3 = 3.3V, $\overline{SHDN}$ = $\overline{STDBY}$ = $\overline{DPRSTP}$ = ILIM = PGDIN = $V_{CC}$, DPRSLPVR = GNDS = PGND = GND, $R_{FB}$ = 4.25kΩ, $V_{CC\_SENSE}$ = $V_{CSP}$ = $V_{CSN}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100 for IMVP-6, D0–D4 = 01000 for GMCH). **$T_A$ = -40°C to +105°C**, unless otherwise specified.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PWM CONTROLLER** | | | | | | |
| Input Voltage Range | | $V_{CC}$, $V_{DD}$ | | 4.5 | 5.5 | V |
| | | $V_{3P3}$ (MAX8796/MAX17401 only) | | 3.0 | 3.6 | |
| DC Output-Voltage Accuracy | | Measured at FB with respect to GNDS; includes load-regulation error (Note 3) | DAC codes from 0.8125V to 1.5000V | -0.75 | +0.75 | % |
| | | | DAC codes from 0.3750V to 0.8000V | -10 | +10 | mV |
| | | | DAC codes from 0 to 0.3625V | -25 | +25 | |
| IMVP-6 Boot Voltage | $V_{BOOT}$ | IMVP-6 (MAX8796/MAX17401 only) | | 1.185 | 1.215 | V |
| GNDS Input Range | | | | -200 | +200 | mV |
| GNDS Gain | $A_{GNDS}$ | $\Delta V_{OUT}/\Delta V_{GNDS}$, -200mV ≤ $V_{GNDS}$ ≤ +200mV | | 0.95 | 1.05 | V/V |
| TIME Voltage | $V_{TIME}$ | $V_{CC}$ = 4.5V to 5.5V, $I_{TIME}$ = 28µA ($R_{TIME}$ = 71.5kΩ) | | 1.98 | 2.02 | V |
| TIME Slew-Rate Accuracy | | $R_{TIME}$ = 71.5kΩ (12.5mV/µs nominal) | | -10 | +10 | % |
| | | $R_{TIME}$ = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal) | | -15 | +15 | |
| | | Soft-start and soft-shutdown; $R_{TIME}$ = 35.7kΩ (3.125mV/µs nominal) to 178kΩ (0.625mV/µs nominal) | | -20 | +20 | |
| | | IMVP-6 slow C4 exit (MAX8796/MAX17401 only)—$\overline{DPRSTP}$ = DPRSLPVR = $V_{CC}$; $R_{TIME}$ = 35.7kΩ (6.25mV/µs nominal) to 178kΩ (1.25mV/µs nominal) | | -20 | +20 | |
| On-Time (Note 4) | $t_{ON}$ | $V_{IN}$ = 12V | $R_{TON}$ = 96.75kΩ | 142 | 192 | ns |
| | | $V_{FB}$ = 1.2V | $R_{TON}$ = 200kΩ | 300 | 366 | |
| | | | $R_{TON}$ = 303.25kΩ | 425 | 575 | |
| Minimum Off-Time | $t_{OFF(MIN)}$ | Measured at DH (Note 4) | | | 400 | ns |
| **BIAS CURRENTS** | | | | | | |
| Quiescent Supply Current ($V_{CC}$) | $I_{CC}$ | Measured at $V_{CC}$, DPRSLPVR = 5V, FB forced above the regulation point | | | 3 | mA |
| Quiescent Supply Current (V3P3) (MAX8796/MAX17401 Only) | $I_{3P3}$ | Measured at V3P3, FB forced within the $\overline{CLKEN}$ power-good window | | | 4µ | A |

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1 (MAX8796/MAX17401), Circuit of Figure 2 (MAX8797), $V_{IN}$ = 12V, $V_{DD}$ = $V_{CC}$ = 5V, V3P3 = 3.3V, $\overline{SHDN}$ = $\overline{STDBY}$ = $\overline{DPRSTP}$ = ILIM = PGDIN = $V_{CC}$, DPRSLPVR = GNDS = PGND = GND, $R_{FB}$ = 4.25kΩ, $V_{CC\_SENSE}$ = $V_{CSP}$ = $V_{CSN}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100 for IMVP-6, D0–D4 = 01000 for GMCH). **$T_A$ = -40°C to +105°C**, unless otherwise specified.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|
| **FAULT PROTECTION** | | | | | | |
| Output Overvoltage-Protection Threshold (MAX8796/MAX8797 Only) | $V_{OVP}$ | Skip mode after output reaches the regulation voltage or PWM mode; measured at FB with respect to typical VID target specified in Table 3 (IMVP-6) and Table 4 (GMCH) | | 240 | 360 | mV |
| | | Soft-start, soft-shutdown, skip mode, and output have not reached the regulation voltage; measured at FB | IMVP-6 (MAX8796 only) | 1.74 | 1.86 | V |
| | | | GMCH (MAX8796 with V3P3 = GND or MAX8797) | 1.49 | 1.61 | |
| Output Undervoltage-Protection Threshold | $V_{UVP}$ | Measured at FB with respect to typical VID target specified in Table 3 (IMVP-6) and Table 4 (GMCH) | | -460 - | 340 | mV |
| IMVP-6 $\overline{CLKEN}$ Startup Delay (Boot Time Period, MAX8796/MAX17401 Only) | $t_{BOOT}$ | IMVP-6: MAX8796/MAX17401 V3P3 = 3.3V; measured from the time when FB reaches the boot target voltage (Note 3); the time needed for FB to reach this target voltage is based on the slew rate set by $R_{TIME}$ | | 20 | 100 | µs |
| PWRGD Startup Delay | | IMVP-6: MAX8796/MAX17401 V3P3 = 3.3V; measured at startup from the time when $\overline{CLKEN}$ goes low | | 3 8 | | ms |
| | | GMCH: MAX8797 or MAX8796/MAX17401 V3P3 = GND; measured from the time when FB reaches the target voltage (Note 3); the time needed for FB to reach this target voltage is based on the slew rate set by $R_{TIME}$ | | 20 | 100 | µs |
| PWRGD and $\overline{CLKEN}$ (MAX8796/MAX17401 IMVP-6 Only) Threshold | | Measured at FB with respect to typical VID target specified in Table 3 (IMVP-6) and Table 4 (GMCH); 50mV hysteresis (typ) | Lower threshold, falling edge (undervoltage) | -360 - | 240 | mV |
| | | | Upper threshold, rising edge (overvoltage) | +140 +260 | | |
| IMVP-6 $\overline{CLKEN}$ Output Low Voltage (MAX8796/MAX17401 Only) | | IMVP-6: MAX8796/MAX17401 V3P3 = 3.3V; $I_{SINK}$ = 3mA | | | 0.4 | V |
| IMVP-6 $\overline{CLKEN}$ Output High Voltage (MAX8796/MAX17401 Only) | | IMVP-6: MAX8796/MAX17401 V3P3 = 3.3V; $I_{SOURCE}$ = 3mA | | V3P3 - 0.4 | | V |
| PWRGD Output Low Voltage | | $I_{SINK}$ = 3mA | | | 0.4 | V |
| $V_{CC}$ Undervoltage Lockout (UVLO) Threshold | $V_{UVLO(VCC)}$ | Rising edge, 65mV typical hysteresis, controller disabled below this level | | 4.0 | 4.5 | V |

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1 (MAX8796/MAX17401), Circuit of Figure 2 (MAX8797), $V_{IN}$ = 12V, $V_{DD}$ = $V_{CC}$ = 5V, V3P3 = 3.3V, $\overline{SHDN}$ = $\overline{STDBY}$ = $\overline{DPRSTP}$ = ILIM = PGDIN = $V_{CC}$, DPRSLPVR = GNDS = PGND = GND, $R_{FB}$ = 4.25kΩ, $V_{CC\_SENSE}$ = $V_{CSP}$ = $V_{CSN}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100 for IMVP-6, D0–D4 = 01000 for GMCH). **$T_A$ = -40°C to +105°C**, unless otherwise specified.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **THERMAL COMPARATOR AND PROTECTION** | | | | | | | |
| $\overline{VRHOT}$ Trip Threshold | | Measured at THRM with respect to $V_{CC}$; falling edge; typical hysteresis = 100mV | | 29 | | 31 | % |
| $\overline{VRHOT}$ Output On-Resistance | $R_{\overline{VRHOT}}$ | Low state | | | | 8 | Ω |
| **VALLEY CURRENT LIMIT AND DROOP** | | | | | | | |
| Current-Limit Threshold Voltage (Positive Adjustable) | $V_{LIMIT}$ | $V_{CSP}$ - $V_{CSN}$ | $V_{TIME}$ - $V_{ILIM}$ = 100mV | 7 | | 13 | mV |
| | | | $V_{TIME}$ - $V_{ILIM}$ = 500mV | 45 | | 55 | |
| Current-Limit Threshold Voltage (Positive Default) | | $V_{CSP}$ - $V_{CSN}$ | IMVP-6 (MAX8796/ MAX17401 only) | 20 | | 25 | mV |
| | | ILIM = $V_{CC}$ | GMCH (MAX8796/ MAX17401 V3P3 = GND or MAX8797) | 15 | | 20 | |
| Current-Limit Threshold Voltage (Negative) Accuracy | $V_{LIMIT(NEG)}$ | $V_{CSP}$ - $V_{CSN}$, nominally -125% of $V_{LIMIT}$ | | -5 | | +5 | mV |
| CSP, CSN Common-Mode Input Range | | | | 0 | | 2 | V |
| Droop Amplifier (GMD) Offset | | ($V_{CSP}$ - $V_{CSN}$) at $I_{FB}$ = 0 | | -1.0 | | +1.0 | mV |
| Droop Amplifier (GMD) Transconductance | | $\Delta I_{FB}/\Delta(V_{CSP} - V_{CSN})$; FB = CSN = 0.45V to 2.0V, and ($V_{CSP}$ - $V_{CSN}$) = -15.0mV to +15.0mV | | 588 | | 612 | µS |
| **POWER MONITOR (PWR)** | | | | | | | |
| Power Monitor Output Voltage for Typical HFM Conditions | $V_{PWR}$ | $V_{CSN}$ - $V_{GNDS}$ = 1.200V | $V_{TIME}$ - $V_{ILIM}$ = 225mV, $V_{CSP}$ - $V_{CSN}$ = 15mV | 1.92 | | 2.08 | V |
| | | $I_{PWR}$ = 0µA | $V_{TIME}$ - $V_{ILIM}$ = 500mV, $V_{CSP}$ - $V_{CSN}$ = 15mV | 0.85 | | 0.95 | |
| Power Monitor Gain Referred to Output Voltage ($V_{CSN}$ - $V_{GNDS}$) | $A_{VPWR}$ | $V_{TIME}$ - $V_{ILIM}$ = 225mV, $V_{CSP}$ - $V_{CSN}$ = 15mV | | 1.583 | | 1.750 | V/V |
| Power Monitor Gain Referred to Current Sense ($V_{CSP}$ - $V_{CSN}$) | $A_{IPWR}$ | $V_{TIME}$ - $V_{ILIM}$ = 225mV, $V_{CSN}$ - $V_{GNDS}$ = 1.200V | | 122 | | 144 | V/V |
| Power Monitor Load Regulation | $\Delta V_{PWR}$ | Measured at PWR with respect to unloaded voltage | Source: $I_{PWR}$ = 0µA to 500µA | -3 | | | mV |

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1 (MAX8796/MAX17401), Circuit of Figure 2 (MAX8797), $V_{IN}$ = 12V, $V_{DD}$ = $V_{CC}$ = 5V, V3P3 = 3.3V, $\overline{SHDN}$ = $\overline{STDBY}$ = $\overline{DPRSTP}$ = ILIM = PGDIN = $V_{CC}$, DPRSLPVR = GNDS = PGND = GND, $R_{FB}$ = 4.25kΩ, $V_{CC\_SENSE}$ = $V_{CSP}$ = $V_{CSN}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100 for IMVP-6, D0–D4 = 01000 for GMCH). **$T_A$ = -40°C to +105°C**, unless otherwise specified.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **GATE DRIVERS** | | | | | | | |
| DH Gate-Driver On-Resistance | $R_{ON(DH)}$ | BST - LX forced to 5V | High state (pullup) | | | 2.5 | Ω |
| | | | Low state (pulldown) | | | 2.0 | |
| DL Gate-Driver On-Resistance | $R_{ON(DL)}$ | | High state (pullup) | | | 2.0 | Ω |
| | | | Low state (pulldown) | | | 0.7 | |
| Internal BST Switch On-Resistance | $R_{BST}$ | $I_{BST}$ = 10mA, $V_{DD}$ = 5V | | | | 20 | Ω |
| **LOGIC AND I/O** | | | | | | | |
| Logic Input High Voltage | $V_{IH}$ | MAX8796/MAX17401: $\overline{SHDN}$, DPRSLPVR, PGDIN; MAX8797: $\overline{SHDN}$, DPRSLPVR; rising edge, typical hysteresis = 250mV | | 2.3 | | | V |
| Logic Input Low Voltage | $V_{IL}$ | MAX8796/MAX17401: $\overline{SHDN}$, DPRSLPVR, PGDIN; MAX8797: $\overline{SHDN}$, DPRSLPVR; falling edge, typical hysteresis = 250mV | | | | 1.0 | V |
| Low-Voltage Logic Input High Voltage | $V_{IHLV}$ | MAX8796/MAX17401: $\overline{DPRSTP}$, D0–D6; MAX8797: $\overline{STDBY}$, D0–D4; rising edge, typical hysteresis = 90mV | | 0.67 | | | V |
| Low-Voltage Logic Input Low Voltage | $V_{ILLV}$ | MAX8796/MAX17401: $\overline{DPRSTP}$, D0–D6; MAX8797: $\overline{STDBY}$, D0–D4; falling edge, typical hysteresis = 90mV | | | | 0.33 | V |

**Note 2:** Limits are 100% production tested at $T_A$ = +25°C. Maximum and minimum limits over temperature are guaranteed by design and characterization.

**Note 3:** The equation for the target voltage $V_{TARGET}$ is:
$V_{TARGET}$ = the slew-rate-controlled version of $V_{DAC}$, where $V_{DAC}$ = 0 for shutdown, $V_{DAC}$ = $V_{BOOT}$ (IMVP-6) or $V_{VID}$ (GMCH) during startup, and $V_{DAC}$ = $V_{VID}$ otherwise (the $V_{VID}$ voltages for all possible VID codes are given in Tables 3 and 4).
In pulse-skipping mode, the output rises by approximately 1.5% when transitioning from continuous conduction to no load.

**Note 4:** On-time and minimum off-time specifications are measured from 50% to 50% at the DH pin, with LX forced to 0V, BST forced to 5V, and a 500pF capacitor from DH to LX to simulate external MOSFET gate capacitance. Actual in-circuit times can be different due to MOSFET switching speeds.

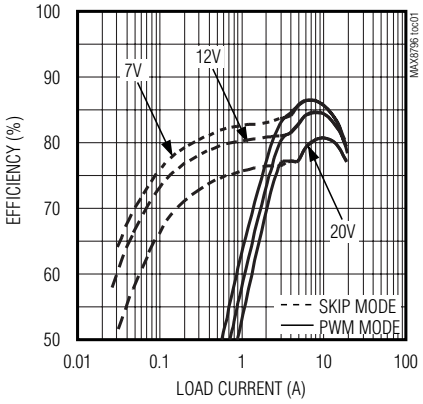
# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller



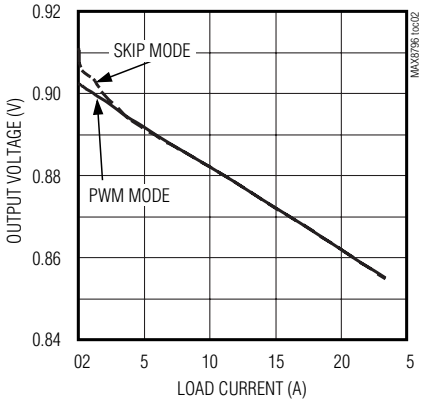
## Typical Operating Characteristics

($T_A$ = +25°C, unless otherwise noted. MAX8796/MAX17401: Circuit of Figure 1 Core 2 Duo ULV. MAX8797: Circuit of Figure 2 Crestline.)

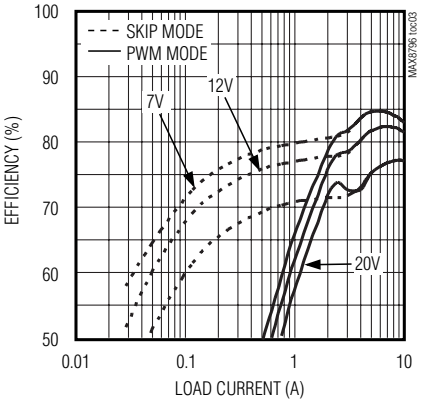
**MAX8796/MAX17401 0.9V OUTPUT EFFICIENCY vs. LOAD CURRENT**



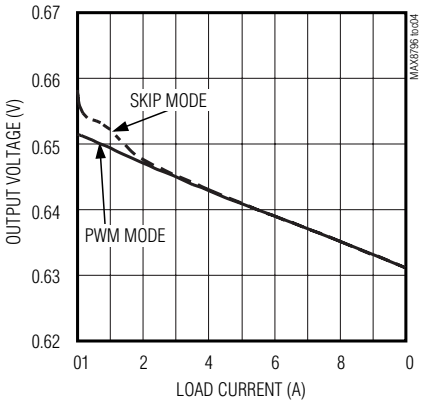

**MAX8796/MAX17401 0.9V OUTPUT VOLTAGE vs. LOAD CURRENT**



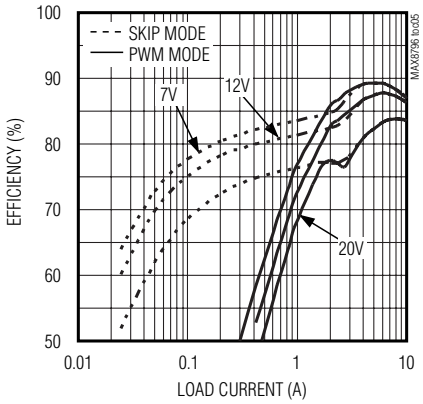

**MAX8796/MAX17401 0.65V OUTPUT EFFICIENCY vs. LOAD CURRENT**



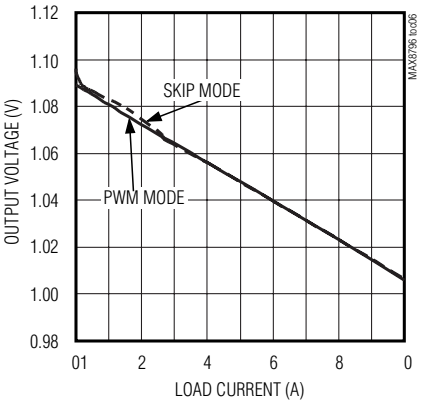

**MAX8796/MAX17401 0.65V OUTPUT VOLTAGE vs. LOAD CURRENT**



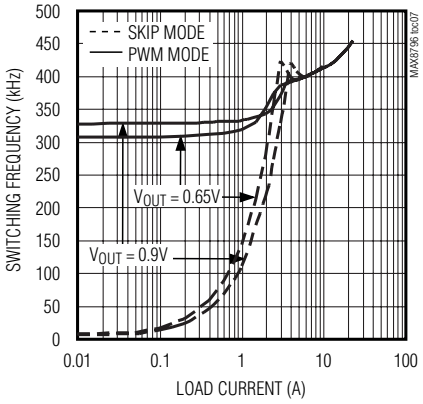

**MAX8797 OUTPUT EFFICIENCY vs. LOAD CURRENT**



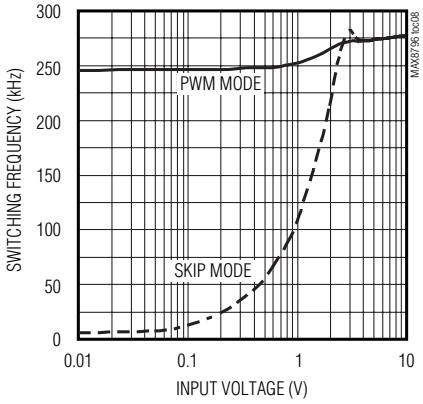

**MAX8797 OUTPUT VOLTAGE vs. LOAD CURRENT**



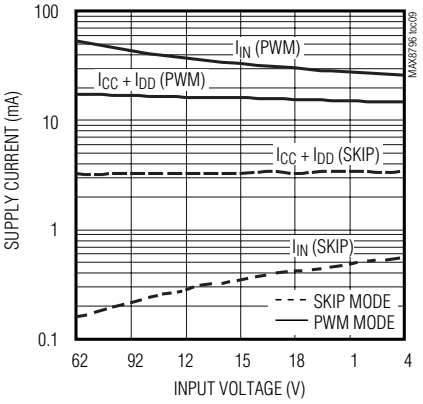

**MAX8796/MAX17401 SWITCHING FREQUENCY vs. LOAD CURRENT**




**MAX8797 SWITCHING FREQUENCY vs. LOAD CURRENT**




**MAX8796/MAX17401 $V_{OUT}$ = 0.9V NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE**

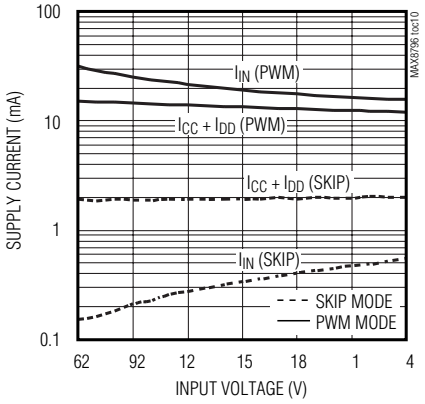


# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

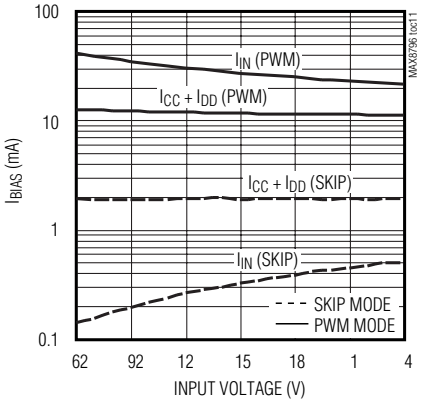
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted. MAX8796/MAX17401: Circuit of Figure 1 Core 2 Duo ULV. MAX8797: Circuit of Figure 2 Crestline.)

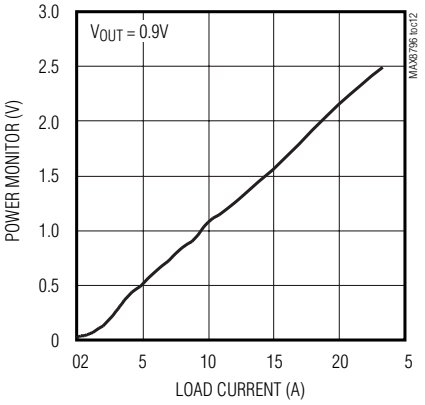
**MAX8796/MAX17401 $V_{OUT}$ = 0.65V NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE**



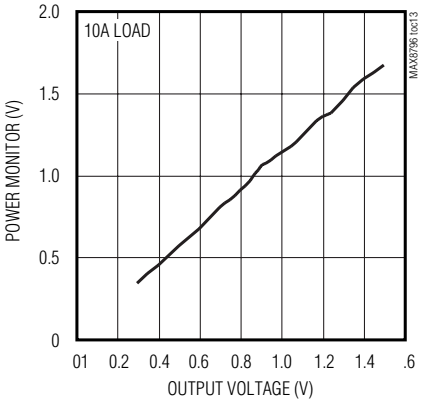

**MAX8797 NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE**



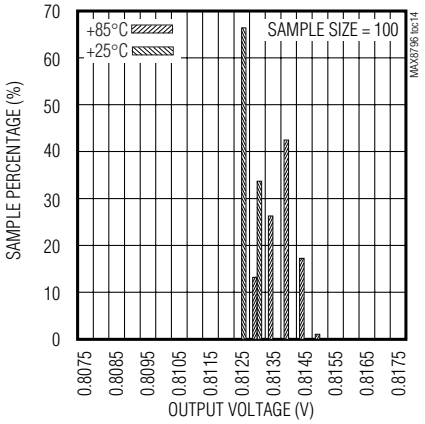

**MAX8796/MAX17401 POWER MONITOR vs. LOAD CURRENT**



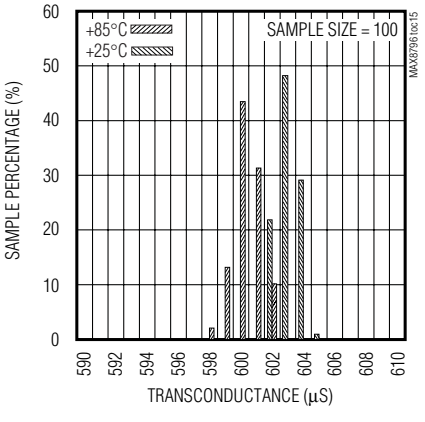

**MAX8796/MAX17401 POWER MONITOR vs. OUTPUT VOLTAGE**




**0.8125V OUTPUT VOLTAGE DISTRIBUTION**



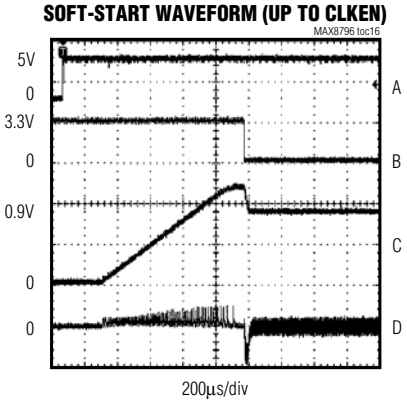

**$G_m$ (FB) TRANSCONDUCTANCE DISTRIBUTION**



## Typical Operating Characteristics (continued)

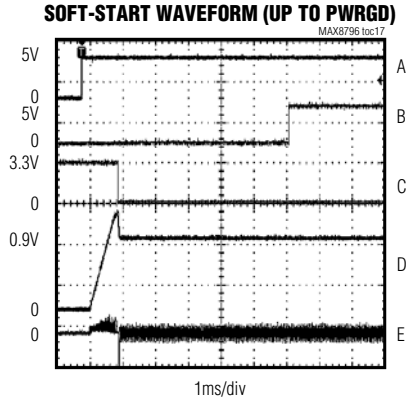
($T_A$ = +25°C, unless otherwise noted. MAX8796/MAX17401: Circuit of Figure 1 Core 2 Duo ULV. MAX8797: Circuit of Figure 2 Crestline.)

**MAX8796/MAX17401 IMVP-6 SOFT-START WAVEFORM (UP TO CLKEN)**



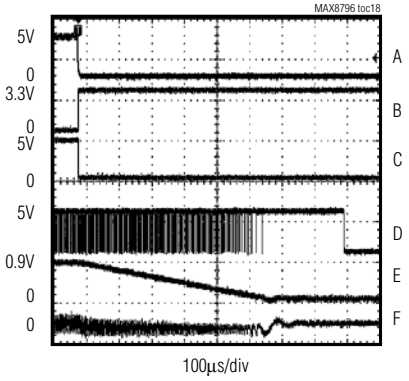

A. $\overline{SHDN}$, 5V/div
B. $\overline{CLKEN}$, 3.3V/div
C. $V_{OUT}$, 500mV/div
D. INDUCTOR CURRENT, 5A/div

**MAX8796/MAX17401 IMVP-6 SOFT-START WAVEFORM (UP TO PWRGD)**



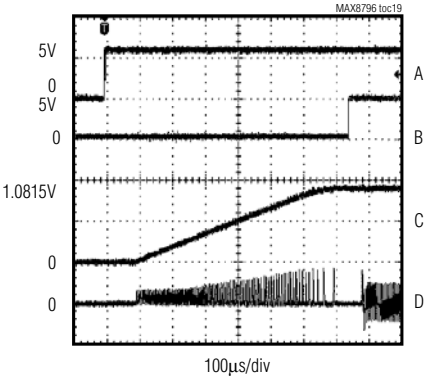

A. PGDIN, 5V/div
B. PWRGD, 5V/div
C. $\overline{CLKEN}$, 3.3V/div
D. $V_{OUT}$, 500mV/div
E. INDUCTOR CURRENT, 5A/div

**MAX8796/MAX17401 IMVP-6 SHUTDOWN WAVEFORM**



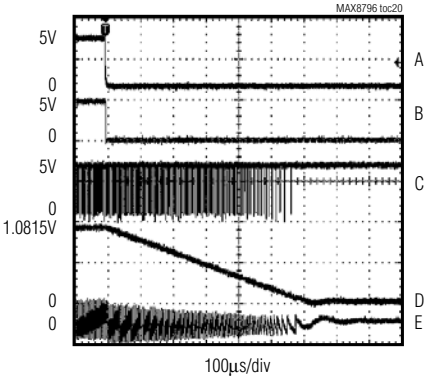

A. $\overline{SHDN}$, 5V/div
B. $\overline{CLKEN}$, 3.3V/div
C. PWRGD, 5V/div
D. $V_{OUT}$, 1V/div
E. DL, 5V/div
F. INDUCTOR CURRENT, 5A/div

**MAX8797 GMCH SOFT-START WAVEFORM**



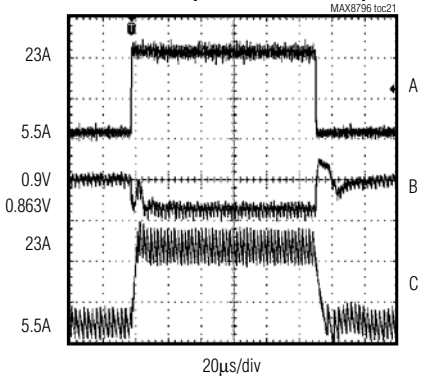

A. $\overline{SHDN}$, 5V/div
B. PWRGD, 5V/div
C. $V_{OUT}$, 500mV/div
D. INDUCTOR CURRENT, 5A/div

**MAX8797 GMCH SHUTDOWN WAVEFORM**




A. $\overline{SHDN}$, 5V/div
B. PWRGD, 5V/div
C. DL, 5V/div
D. $V_{OUT}$, 500mV/div
E. INDUCTOR CURRENT, 5A/div

**MAX8796/MAX17401 LOAD-TRANSIENT RESPONSE (IMVP-6 HFM MODE)**



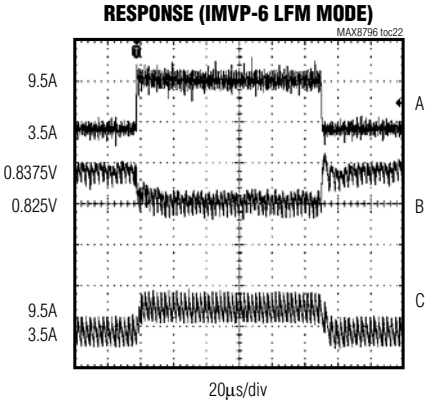

A. $I_{OUT}$ = 5.5 TO 23A, 10A/div
B. $V_{OUT}$, 50mV/div
C. INDUCTOR CURRENT, 10A/div

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

## Typical Operating Characteristics (continued)

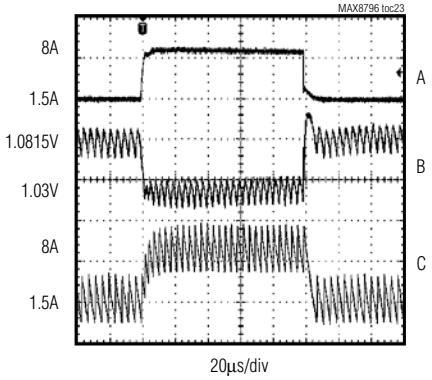
($T_A$ = +25°C, unless otherwise noted. MAX8796/MAX17401: Circuit of Figure 1 Core 2 Duo ULV. MAX8797: Circuit of Figure 2 Crestline.)

**MAX8796/MAX17401 LOAD-TRANSIENT RESPONSE (IMVP-6 LFM MODE)**



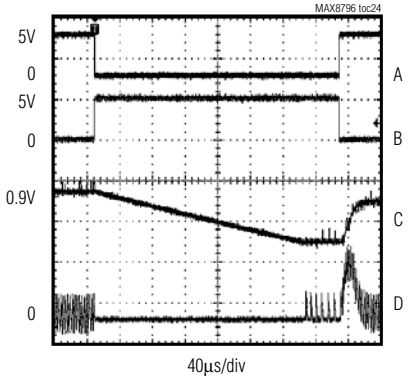

A. $I_{OUT}$ = 3.5A TO 9.5A, 5A/div
B. $V_{OUT}$, 20mV/div
C. INDUCTOR CURRENT, 10A/div

**MAX8797 LOAD-TRANSIENT RESPONSE**



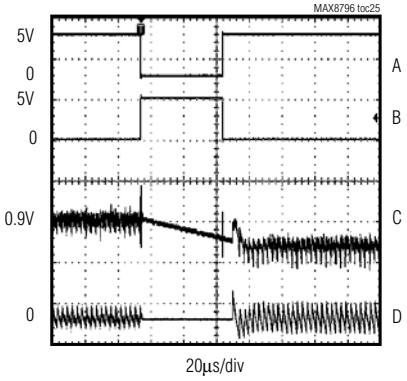

A. $I_{OUT}$ = 1.5A TO 8A, 5A/div
B. $V_{OUT}$, 50mV/div
C. INDUCTOR CURRENT, 5A/div

**ENTERING DEEPER SLEEP EXITING TO LFM**



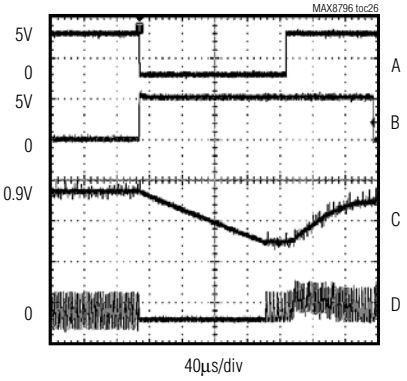

A. $\overline{DPRSTP}$, 5V/div
B. DPRSLPVR, 5V/div
$I_{OUT}$ = 1A
C. $V_{OUT}$, 200mV/div
D. INDUCTOR CURRENT, 10A/div

**ENTERING DEEPER SLEEP EXITING TO NEAREST VID**



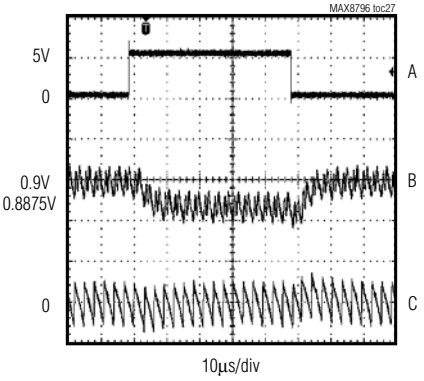

A. $\overline{DPRSTP}$, 5V/div
B. DPRSLPVR, 5V/div
$I_{OUT}$ = 0.3A
C. $V_{OUT}$, 20mV/div
D. INDUCTOR CURRENT, 10A/div

**ENTERING DEEPER SLEEP EXITING TO LFM**




A. $\overline{DPRSTP}$, 5V/div
B. DPRSLPVR, 5V/div
$I_{OUT}$ = 2A
C. $V_{OUT}$, 200mV/div
D. INDUCTOR CURRENT, 10A/div

**D0 12.5mV DYNAMIC VID CODE CHANGE**

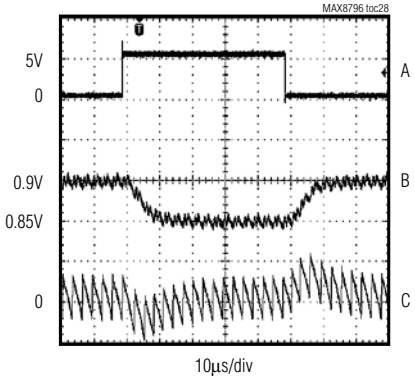



A. D0, 5V/div
B. $V_{OUT}$, 20mV/div
C. INDUCTOR CURRENT, 2A/div

## Typical Operating Characteristics (continued)

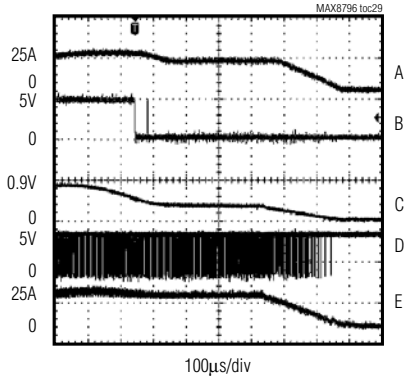
($T_A$ = +25°C, unless otherwise noted. MAX8796/MAX17401: Circuit of Figure 1 Core 2 Duo ULV. MAX8797: Circuit of Figure 2 Crestline.)

**D2 50mV DYNAMIC VID CODE CHANGE**



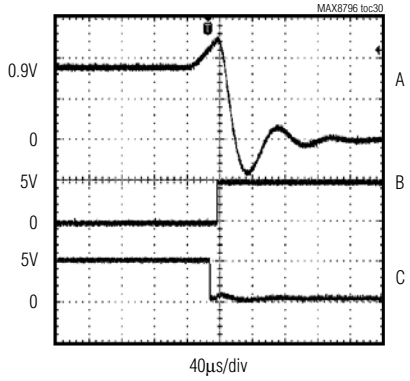

A. D2, 5V/div
B. $V_{OUT}$, 50mV/div
C. INDUCTOR CURRENT, 2A/div

**OUTPUT OVERLOAD WAVEFORM**



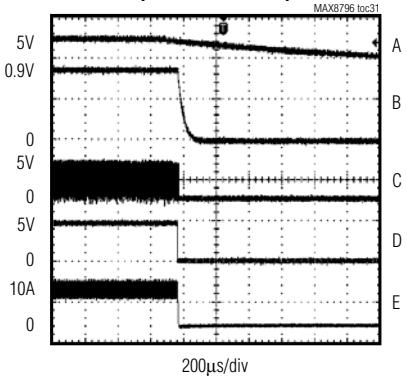

A. LOAD CURRENT, 25A/div
B. PGOOD, 5V/div
C. $V_{OUT}$, 1V/div
D. DL, 5V/div
E. INDUCTOR CURRENT, 25A/div

**OUTPUT OVERVOLTAGE WAVEFORM**



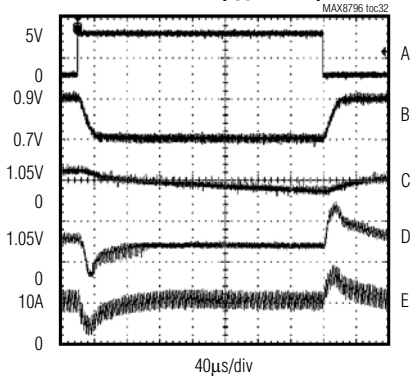

A. $V_{OUT}$, 500mV/div
B. DL, 5V/div
C. PWRGD, 5V/div

**BIAS SUPPLY REMOVAL (UVLO RESPONSE)**




A. 5V BIAS SUPPLY, 5V/div
B. $V_{OUT}$, 500mV/div
C. DL, 5V/div
D. PGOOD, 5V/div
E. INDUCTOR CURRENT, 10A/div

**POWER MONITOR - VID TRANSITION RESPONSE ($I_{OUT}$ = 10A)**




A. D4, 5V/div
B. $V_{OUT}$, 200mV/div
C. $P_{OUT}$ WITH RC FILTER, 1V/div
D. $P_{OUT}$, 1V/div
E. INDUCTOR CURRENT, 10A/div

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX8796/ MAX17401 | MAX8797 | | |
| 1 | 1 | PWR | Power Monitor Output. The voltage on PWR is directly proportional to the amount of power being delivered to support the load: $V_{PWR} = \frac{K_{PWR}(V_{CSN} - V_{GNDS})(V_{CSP} - V_{CSN})}{(V_{TIME} - V_{ILIM})}$ where $K_{PWR}$ = 25 is the power monitor scale factor. The MAX8796/MAX8797/MAX17401 pull PWR to ground when the controller is disabled. |
| 2 | 2 | GNDS | Remote Ground-Sense Input. Connect directly to the CPU or GMCH $V_{SS}$ sense pin (ground sense) or directly to the ground connection of the load. GNDS internally connects to a transconductance amplifier that adjusts the feedback voltage, compensating for voltage drops between the regulator's ground and the processor's ground. |
| 3 | 3 | FB | Remote-Sense Feedback Input and Voltage-Positioning Transconductance Amplifier Output. Connect a resistor $R_{FB}$ between FB and the output remote sense ($V_{CC\_SENSE}$) to set the steady-state droop based on the voltage-positioning gain requirement: $R_{FB} = R_{DROOP} / (R_{SENSE} \times G_{MD})$ where $R_{DROOP}$ is the desired voltage-positioning slope, $G_{MD}$ = 600µS typ and $R_{SENSE}$ is the current-sense resistance with respect to the CSP-to-CSN current-sense inputs. See the *Current Sense* section for details on designing with sense resistors or inductor DCR sensing. Shorting FB directly to the output effectively disables voltage positioning, but impacts the stability requirements. Designs that disable voltage positioning require a higher minimum output capacitance ESR to maintain stability (see the *Output Capacitor Selection* section). FB enters a high-impedance state in shutdown. |
| 4 | 4 | CSN | Negative Inductor Current-Sense Input. Connect CSN to the negative terminal of the inductor current-sensing resistor or directly to the negative terminal of the inductor if the lossless DCR sensing method is used (see Figure 4). The MAX8796/MAX8797/MAX17401 also use CSN as the voltage input to the power monitor. Under $V_{CC}$ UVLO conditions and after soft-shutdown is completed, CSN is internally pulled to GND through a 10Ω FET to discharge the output. |
| 5 | 5 | CSP | Positive Inductor Current-Sense Input. Connect CSP to the positive terminal of the inductor current-sensing resistor or directly to the positive terminal of the filtering capacitor used when the lossless DCR sensing method is used (see Figure 4). |
| 6 | — | $\overline{DPRSTP}$ | Deeper Stop Input and Slew-Rate Control Signal (MAX8796/MAX17401 Only). This 1V logic input signal from the system is usually the logical complement of the DPRSLPVR signal. However, there is a special condition during C4 exit when both $\overline{DPRSTP}$ and DPRSLPVR could temporarily be simultaneously high. If this happens, the MAX8796/MAX17401 reduce the slew rate to 1/4 the nominal ($R_{TIME}$-based) slew rate for the duration of this condition. The slew rate returns to nominal when this condition is exited. Note that only DPRSLPVR (and not $\overline{DPRSTP}$) determines the mode of operation (PWM vs. skip). |

| DPRSLPVR | $\overline{DPRSTP}$ | Functionality |
|---|---|---|
| 0 | X | Nominal slew rate, 1-phase forced-PWM mode (DPRSLPVR low ➔ $\overline{DPRSTP}$ is ignored) |
| 1 | 0 | Nominal slew rate, 1-phase skip mode |
| 1 | 1 | Slew rate reduced to 1/4 of nominal, 1-phase skip mode |

The $\overline{DPRSTP}$ state is ignored during soft-start and shutdown. The MAX8796/MAX8797/MAX17401 always use 1/8 of nominal slew rate during startup to minimize the surge current. During shutdown, the controller always uses 1/8 of the nominal slew rate to provide a soft-shutdown to avoid excessive output ringing below ground.

## Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX8796/ MAX17401 | MAX8797 | | |
| 7 | 6 | DPRSLPVR | Deeper Sleep Status Signal—Pulse-Skipping and Slew-Rate Control Input. The DPRSLPVR signal indicates the IMVP-6 power usage and sets the operating mode of the MAX8796/ MAX8797/MAX17401. When the system forces DPRSLPVR high, the MAX8796/MAX8797/ MAX17401 immediately enter automatic pulse-skipping mode. The controller returns to continuous forced-PWM mode when DPRSLPVR is pulled low and the output is in regulation. DPRSLPVR determines the operating mode and output-voltage-transition slew rate as shown in the truth table below:<br>DPRSLPVR / $\overline{DPRSTP}$ / Functionality<br>0 / X / Nominal slew rate, 1-phase forced PWM mode (DPRSLPVR low ➔ $\overline{DPRSTP}$ is ignored)<br>1 / 0 / Nominal slew rate, 1-phase skip mode<br>1 / 1 / Slew rate reduced to 1/4 of nominal, 1-phase skip mode<br>The DPRSLPVR state is ignored during soft-start and shutdown. The MAX8796/MAX8797/ MAX17401 always use pulse-skipping mode during startup to ensure a monotonic power-up. During shutdown, the controller always uses forced-PWM mode so the output can be actively discharged. |
| 8 | 7 | THRM | Comparator Input for Thermal Protection. THRM connects to the positive input of an internal comparator. The comparator's negative input connects to an internal resistive voltage-divider that accurately sets the THRM threshold to 30% of the $V_{CC}$ voltage. Connect the output of a resistor and thermistor divider (between $V_{CC}$ and GND) to THRM with the values selected so the voltage at THRM falls below 30% of $V_{CC}$ (1.5V when $V_{CC}$ = 5V) at the desired high temperature. |
| 9 | 8 | TON | Switching Frequency Setting Input. An external resistor ($R_{TON}$) between the input power source and TON sets the switching frequency ($f_{SW} = 1/t_{SW}$) according to the following equation used to determine the nominal switching period:<br>$t_{SW} = 16.3pF \times (R_{TON} + 6.5k\Omega)$<br>TON enters high impedance in shutdown to reduce the input quiescent current. If the TON current is less than 10µA, the MAX8796/MAX8797/MAX17401 disable the controller, set the TON open fault latch, and pull DL and DH low. |
| 10 | 9 | PWRGD | Open-Drain Power-Good Output. The MAX8796/MAX8797/MAX17401 force PWRGD low when $\overline{SHDN}$, PGDIN, or $\overline{STDBY}$ are pulled low. After the controller is properly powered up, PWRGD becomes a high-impedance output as long as the feedback voltage is in regulation and the startup blanking time has expired:<br>IMVP-6 (MAX8796/MAX17401 V3P3 = 3.3V): PWRGD becomes active 5ms after the MAX8796/ MAX17401 pull $\overline{CLKEN}$ low. The MAX8796/MAX17401 pull PWRGD low when shut down ($\overline{SHDN}$ = GND) or the power-good input (PGDIN = GND) is pulled low, and during the startup and shutdown transitions.<br>GMCH (MAX8797 or MAX8796/MAX17401 V3P3 = GND): PWRGD becomes active 60µs after the soft-start sequence has been completed. The MAX8796/MAX8797/MAX17401 pull PWRGD low when shutdown ($\overline{SHDN}$ = GND) or standby ($\overline{STDBY}$ = GND) are pulled low, and during the startup and shutdown transitions.<br>The PWRGD upper threshold is blanked during any downward output-voltage transition that occurs when the MAX8796/MAX8797/MAX17401 are in skip mode (DPRSLPVR pulled high). PWRGD remains blanked until the transition-related PWRGD blanking period expires and the controller detects the output is in regulation (error amplifier edge occurs).<br>**Note:** The pullup resistance on PWRGD causes additional shutdown current. |

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

## Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX8796/ MAX17401 | MAX8797 | | |
| 11 | 10 | $\overline{SHDN}$ | Shutdown Control Input. Connect to $V_{CC}$ for normal operation. Connect to ground to put the controller into the low-power 1µA (max) shutdown state. During startup, the controller ramps up the output voltage at 1/8 the slew rate set by the TIME resistor to the target voltage defined by the application circuit:<br>IMVP-6 (MAX8796/MAX17401 V3P3 = 3.3V) startup target = the 1.2V boot voltage GMCH (MAX8797 or MAX8796/MAX17401 V3P3 = GND) startup target = voltage set by the VID inputs<br>During the shutdown transition, the MAX8796/MAX8797/MAX17401 softly ramp down the output voltage at 1/8 the slew rate set by the TIME resistor. Forcing $\overline{SHDN}$ to 11V ~ 13V disables overvoltage protection (OVP), undervoltage protection (UVP), and thermal shutdown, and clears the fault latches. |
| 12 | — | $\overline{CLKEN}$ | IMVP-6 Clock Enable Output (MAX8796/MAX17401 Only). $\overline{CLKEN}$ uses CMOS push-pull logic so no external pullup resistor is necessary. This active-low logic output indicates when the feedback voltage is in regulation. The MAX8796/MAX17401 force $\overline{CLKEN}$ low during dynamic VID transitions and for an additional 20µs after the VID transition is completed. $\overline{CLKEN}$ is the inverse of PWRGD, except for the 5ms PWRGD startup delay period after $\overline{CLKEN}$ is pulled low. See the startup timing diagram (Figure 11). The $\overline{CLKEN}$ upper threshold is blanked during any downward output voltage transition that happens when the MAX8796/MAX17401 are in skip mode, and stays blanked until the transition-related PWRGD blanking period is complete and the output reaches regulation. |
| 13 | — | V3P3 | 3.3V $\overline{CLKEN}$ Input Supply (MAX8796/MAX17401 Only). V3P3 input supplies the $\overline{CLKEN}$ CMOS push-pull logic output. Connect to the system's standard 3.3V supply voltage before $\overline{SHDN}$ is pulled high for proper IMVP-6 operation.<br>Connect V3P3 = GND to select the Intel GMCH VID code and feature set. |
| 14–20 | 11–15 | D0–D6 (GMCH: D0–D4) | Low-Voltage (1.0V Logic) VID DAC Code Inputs. The D0–D6 (IMVP-6) or D0–D4 (GMCH) inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the CPU. The output voltage is set by the VID code indicated by the logic level voltages on D0–D6 (IMVP-6, see Table 3) or D0–D4 (GMCH, see Table 4).<br>The MAX8796/MAX17401 can be configured to support either IMVP-6 (V3P3 = 3.3V) or GMCH (V3P3 = GND) applications. When configured for the GMCH code set, pin 14 to pin 18 of the MAX8796/MAX17401 serve as the D0 to D4 VID inputs (respectively) and pin 19 provides the standby function. |
| — | 16 | $\overline{STDBY}$ | GMCH Standby Logic Input (GMCH). $\overline{STDBY}$ is low-voltage logic input (1V logic) similar to those used on the VID inputs. When $\overline{STDBY}$ is pulled low, the GMCH controller enters standby mode and actively slews down the output to 0V at 1/8 the slew rate set by the TIME resistance. Once the output is discharged, the controller enters a high-impedance output state (DH and DL pulled low). When $\overline{STDBY}$ is forced high, the controller exits standby mode (while in skip mode) and slews the output voltage to the target voltage set by the VID code at 1/4 the slew rate set by the TIME resistance.<br>$\overline{SHDN}$ always overrides the $\overline{STDBY}$ signal.<br>When the MAX8796/MAX17401 are configured for the GMCH code set (V3P3 = GND), pin 14 to pin 18 of the MAX8796/MAX17401 serve as the D0 to D4 GMCH VID inputs (respectively) and pin 19 provides the standby function. |
| 21 | 17 | PGND | Power Ground. Ground connection for the DL driver. |

## Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX8796/ MAX17401 | MAX8797 | | |
| 22 | 18 | DL | Low-Side Gate-Driver Output. DL swings from $V_{DD}$ to PGND. DL is forced low in shutdown. DL is forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that might be present. DL is forced low in skip mode after detecting an inductor current zero crossing. |
| 23 | 19 | $V_{DD}$ | Driver-Supply Voltage Input. $V_{DD}$ supplies power to the low-side gate driver (DL) and to the internal BST switch used to refresh the BST capacitor. Connect $V_{DD}$ to the 4.5V to 5.5V system supply voltage. Bypass $V_{DD}$ to PGND with a 1µF or greater ceramic capacitor. |
| 24 | 20 | BST | Boost Flying Capacitor Connection. BST provides the upper supply rail for the DH high-side gate driver. An internal switch between $V_{DD}$ and BST charges the flying capacitor while the low-side MOSFET is on (DL pulled high and LX pulled to ground). |
| 25 | 21 | LX | Inductor Connection. LX serves as the lower supply rail for the DH high-side gate driver. The MAX8796/MAX8797/MAX17401 also use LX as the input to the zero-crossing comparator. |
| 26 | 22 | DH | High-Side Gate-Driver Output. DH swings from LX to BST. The controller pulls DH low in shutdown. |
| — | 23 | GND | Analog Ground. Connect to the exposed backside pad and low-current analog ground terminations. |
| 27 | — | PGDIN | IMVP-6 Power-Good Logic Input (MAX8796/MAX17401 Only). PGDIN indicates the power status of other system rails used to power the chipset and CPU VCCP supplies. For the IMVP-6 (V3P3 = 3.3V), the MAX8796/MAX17401 power up and remain at the boot voltage ($V_{BOOT}$) as long as PGDIN remains low. When PGDIN is forced high, the MAX8796/MAX17401 transition the output to the voltage set by the VID code, and $\overline{CLKEN}$ is allowed to go low.<br>If PGDIN is pulled low at any time, the MAX8796/MAX17401 immediately force $\overline{CLKEN}$ high and PWRGD low and sets the output to the boot voltage. The output remains at the boot voltage until the system either disables the controller or until PGDIN goes high again. PGDIN is only active for IMVP-6 configurations (V3P3 = 3.3V). For GMCH applications (V3P3 = GND), the PGDIN input is blanked high. |
| 28 | 24 | $\overline{VRHOT}$ | Thermal Comparator's Open-Drain Output. The comparator pulls $\overline{VRHOT}$ low when the voltage at THRM drops below 30% of $V_{CC}$ (1.5V with 5V x $V_{CC}$). $\overline{VRHOT}$ is high impedance in shutdown. |
| 29 | 25 | TIME | Slew-Rate Adjustment. TIME regulates to 2.0V and the load current determines the slew rate of the internal error-amplifier target. The sum of the resistance between TIME and GND ($R_{TIME}$) determines the nominal slew rate:<br>SLEW RATE = (12.5mV/µs) x (71.5kΩ / $R_{TIME}$)<br>The guaranteed $R_{TIME}$ range is between 35.7kΩ and 178kΩ. This nominal slew rate applies to VID transitions and to the transition from boot mode to VID. If the VID DAC inputs are clocked, the slew rate for all other VID transitions is set by the rate at which they are clocked, up to a maximum slew rate equal to the nominal slew rate defined above.<br>The startup and shutdown slew rates are always 1/8 of nominal slew rate to minimize surge currents.<br>For IMVP-6 (MAX8796/MAX17401 V3P3 = 3.3V), if DPRSLPVR and $\overline{DPRSTP}$ are both high, then the slew rate is reduced to 1/4 of nominal.<br>For GMCH (MAX8797 or MAX8796/MAX17401 V3P3 = GND), the slew rate for wakeup from standby is 1/4 of nominal, but the slew rate when entering standby is 1/8 of nominal. |

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

## Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX8796/ MAX17401 | MAX8797 | | |
| 30 | 26 | ILIM | Valley Current-Limit Adjustment Input. The valley current-limit threshold voltage at CSP to CSN equals precisely 1/10 of the differential TIME to ILIM voltage over a 0.1V to 0.5V range (10mV to 50mV current-sense range). The negative current-limit threshold is nominally -125% of the corresponding valley current-limit threshold.<br>Connect ILIM directly to $V_{CC}$ to set the default current-limit threshold setting of 22.5mV nominal for IMVP-6 (MAX8796/MAX17401 V3P3 = 3.3V) and 17.5mV nominal for GMCH (MAX8797 and MAX8796/MAX17401 V3P3 = GND). |
| 31 | 27 | $V_{CC}$ | Analog Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to GND with 1µF minimum. |
| 32 | 28 | CCV | Integrator Capacitor Connection. Connect a capacitor ($C_{CCV}$) from CCV to GND to set the integration time constant. Choose the capacitor value according to:<br>$16\pi \times [C_{CCV} / G_{m(CCV)}] \times f_{SW} >> 1$<br>where $G_{m(CCV)}$ = 320µS (max) is the integrator's transconductance and $f_{SW}$ is the switching frequency set by the $R_{TON}$ resistance.<br>The integrator is internally disabled during any downward output voltage transition that occurs in pulse-skipping mode, and remains disabled until the transition blanking period expires and the output reaches regulation (error amplifier transition detected). |
| — | — | PAD (GND) | Analog Ground and Exposed Pad (Back Side). Internally connected to GND. Connect to the ground plane through a thermally enhanced via. **Note: For the MAX8796/MAX17401, this is the only GND pin**. |

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller



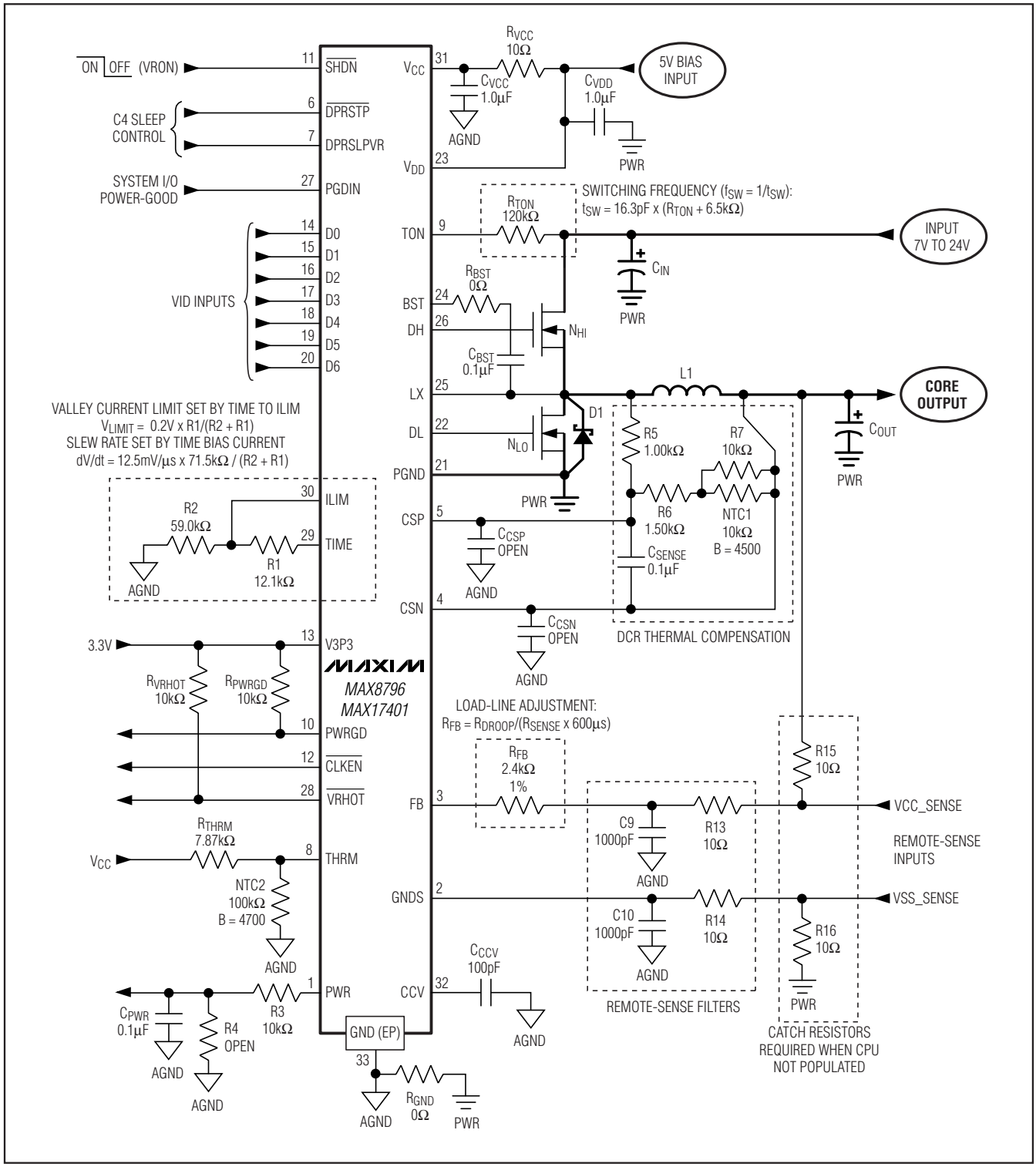



*Figure 1. MAX8796/MAX17401 IMVP-6 Application Circuit*

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

## Table 1. IMVP-6 Component Selection

| DESIGN PARAMETERS | SANTA ROSA CORE 2 DUO LV | SANTA ROSA CORE 2 DUO ULV | CENTRINO ULV CORE SOLO | SILVERTHORNE UMPC/LPIA CORE |
|---|---|---|---|---|
| Input Voltage Range | 7V to 20V | 7V to 20V | 7V to 20V | 4.5V to 8.0V |
| Maximum Load Current | 23A (30A OCP) | 17A (21A OCP) | 8A (10A OCP) | 4A (5A OCP) |
| Transient Load Current | 19A (10A/µs) | 14A (10A/µs) | 5.5A (5A/µs) | 3.6A (2.5A/µs) |
| Load Line | 2.1mV/A | 2.1mV/A | 5.1mV/A | 5.7mV/A |
| **COMPONENTS** | | | | |
| TON Resistance ($R_{TON}$) | 200kΩ ($f_{SW}$ = 300kHz) | 150kΩ ($f_{SW}$ = 400kHz) | 120kΩ ($f_{SW}$ = 500kHz) | 120kΩ ($f_{SW}$ = 500kHz) |
| Inductance (L) | NEC/TOKIN MPC1055LR36 0.36µH, 32A, 0.8mΩ | NEC-TOKIN MPC0730LR20 1µH, 25A, 1.0mΩ | Vishay-Dale IHLP-2525CZ-07 0.47µH, 17A, 3.86mΩ | NEC-TOKIN MPLC0525L1R0 1µH, 7A, 14mΩ |
| High-Side MOSFET ($N_H$) | Siliconix Si4386DY 7.8mΩ/9.5mΩ (typ/max) | Fairchild FDS6298 9.4mΩ/12mΩ (typ/max) | Siliconix Si4386DY 7.8mΩ/9.5mΩ (typ/max) | Fairchild FDS6982S NH: 28mΩ/35mΩ (typ/max) NL: 17mΩ/22mΩ (typ/max) |
| Low-Side MOSFET ($N_L$) | 2x Siliconix Si4642DY 3.9mΩ/4.7mΩ (typ/max) | Fairchild FDS8670 4.2mΩ/5.0mΩ (typ/max) | Siliconix Si4642DY 3.9mΩ/4.7mΩ (typ/max) | |
| Output Cap ($C_{OUT}$) | Panasonic 4x 330µF, 6mΩ, 2.5V EEFSX0D0D331XR 32x 10µF, 6V ceramic (0805) | 6x 100µF, 4V ceramic (1210) 32x 10µF, 6V ceramic (0805) | SANYO 2x 220µF, 7mΩ, 2.0V 2TPF220M7 12x 10µF, 6V ceramic (0805) | 2x 47µF, 6V ceramic (1210) 2x 10µF, 6V ceramic (0805) |
| Input Cap ($C_{IN}$) | 4x 10µF, 25V ceramic (1210) | 3x 10µF, 25V ceramic (1210) | 2x 10µF, 25V ceramic (1210) | 1x 10µF, 16V ceramic (1206) |
| TIME/ILIM Resistance (R1) | 6.19kΩ | 4.42kΩ | 12.1kΩ | 17.8kΩ |
| ILIM/GND Resistance (R2) | 64.9kΩ | 66.5kΩ | 59.0kΩ | 53.6kΩ |
| FB Resistance ($R_{FB}$) | 4.99kΩ | 4.42kΩ | 2.49kΩ | 1.05kΩ |
| LX/CSP Resistance (R5) | 1.00kΩ | 2.20kΩ | 1.00kΩ | 1.13kΩ |
| CSP/CSN Series Resistance (R6) | 1.50kΩ | 2.37kΩ | 1.50kΩ | 2.26kΩ |
| Parallel NTC Resistance (R7) | 10.0kΩ | 15kΩ | 10.0kΩ | Open |
| DCR Sense NTC (NTC1) | 10kΩ NTC B = 3380 TDK NTCG163JH103F | 10kΩ NTC B = 3380 TDK NTCG163JH103F | 10kΩ NTC B = 3380 TDK NTCG163JH103F | Short |
| DCR Sense Capacitance ($C_{SENSE}$) | 0.47µF, 6V ceramic (0805) | 0.1µF, 6V ceramic (0603) | 0.1µF, 6V ceramic (0603) | 0.1µF, 6V ceramic (0603) |

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller



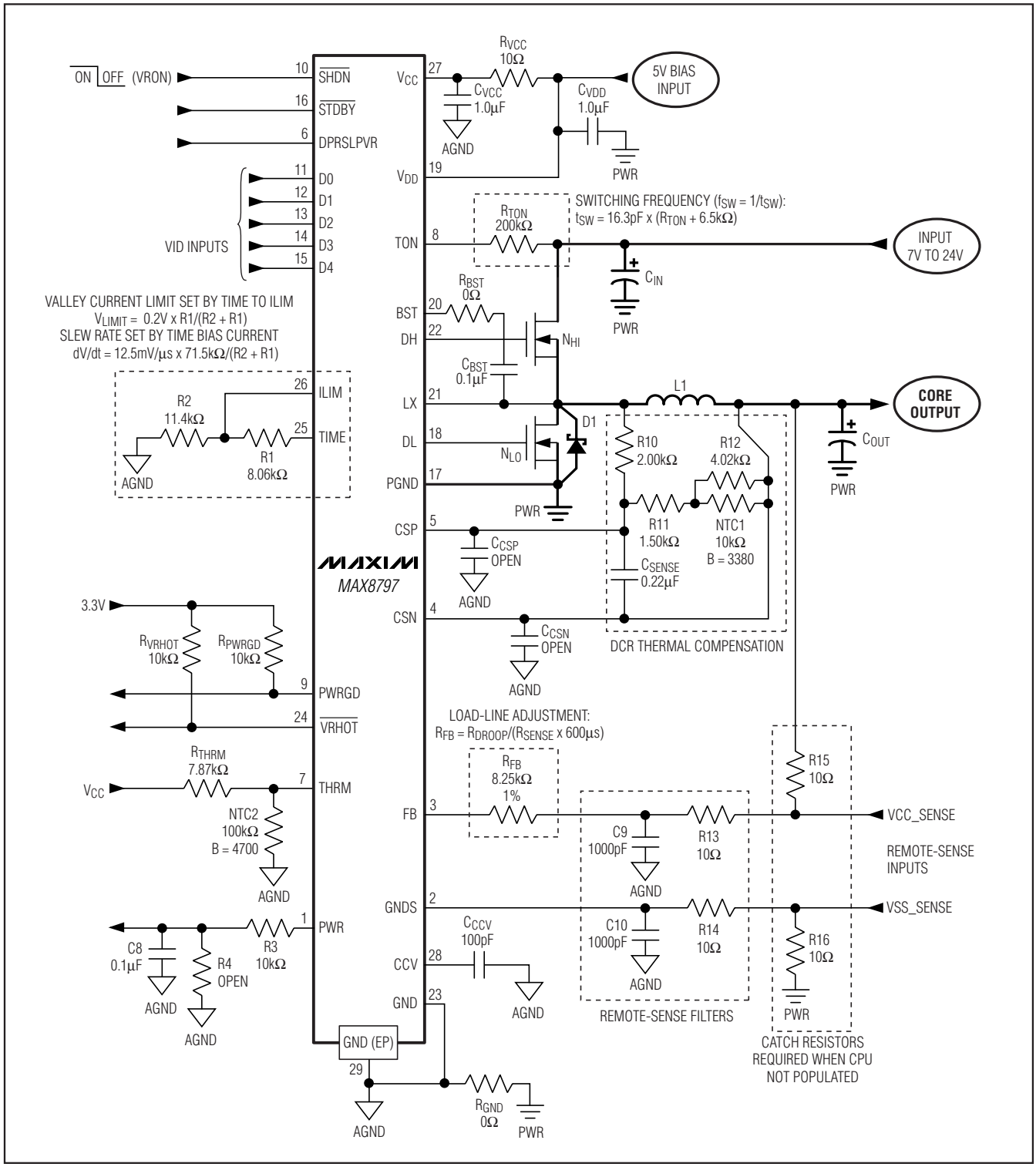



*Figure 2. MAX8797 GMCH Application Circuit*

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

**Table 2. GMCH Component Selection**

| DESIGN PARAMETERS | CRESTLINE | CANTIGA |
|---|---|---|
| Input Voltage Range | 7V to 20V | 7V to 20V |
| Maximum Load Current | 8A<br>(10A OCP) | 10A<br>(12A OCP) |
| Transient Load Current | 7A<br>(5A/µs) | 8A<br>(5A/µs) |
| Load Line | 7.8mV/A | 7.5mV/A |
| **COMPONENTS** | | |
| TON Resistance ($R_{TON}$) | 200kΩ<br>($f_{SW}$ = 300kHz) | 200kΩ<br>($f_{SW}$ = 300kHz) |
| Inductance (L) | NEC/TOKIN MPC0750LR60<br>0.56µH, 17A, 2.30mΩ | NEC/TOKIN MPC0750LR60<br>0.56µH, 17A, 2.30mΩ |
| High-Side MOSFET ($N_H$) | Fairchild FDS8690<br>8.6mΩ/11.4mΩ (typ/max) | Fairchild FDS8690<br>8.6mΩ/11.4mΩ (typ/max) |
| Low-Side MOSFET ($N_L$) | Fairchild FDS8660S<br>2.6mΩ/3.5mΩ (typ/max) | Fairchild FDS8660S<br>2.6mΩ/3.5mΩ (typ/max) |
| Output Cap ($C_{OUT}$) | 2x 330µF, 12mΩ, 2.5V<br>SANYO 2R5TPE330MCC2<br>6x 10µF, 6V ceramic (0805) | 2x 330µF, 12mΩ, 2.5V<br>SANYO 2R5TPE330MCC2<br>6x 10µF, 6V ceramic (0805) |
| Input Cap ($C_{IN}$) | 2x 10µF, 25V ceramic (1210) | 2x 10µF, 25V ceramic (1210) |
| TIME/ILIM Resistance (R1) | 7.15kΩ | 8.06kΩ |
| ILIM/GND Resistance (R2) | 61.9kΩ | 61.9kΩ |
| FB Resistance ($R_{FB}$) | 8.25kΩ | 8.25kΩ |
| LX/CSP Resistance (R10) | 2.00kΩ | 2.00kΩ |
| CSP/CSN Series Resistance (R11) | 1.50kΩ | 1.50kΩ |
| Parallel NTC Resistance (R12) | 4.02kΩ | 4.02kΩ |
| DCR Sense NTC (NTC1) | 10kΩ NTC B = 3380<br>TDK NTCG163JH103F | 10kΩ NTC B = 3380<br>TDK NTCG163JH103F |
| DCR Sense Capacitance ($C_{SENSE}$) | 0.1µF, 6V ceramic (0603) | 0.1µF, 6V ceramic (0603) |

## Detailed Description

### Free-Running, Constant On-Time Controllers with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator with voltage feed-forward (Figure 3). This architecture relies on the output filter capacitor's ESR and the load regulation to provide the proper current-mode compensation, so the resulting feedback ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage, and directly proportional to the feedback voltage (see the *On-Time One-Shot* section). Another one-shot sets a minimum off-time. The on-time one-shot triggers when the error comparator goes low (the feedback voltage drops below the target voltage), the inductor current is below the valley current-limit threshold, and the minimum off-time one-shot times out.

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller



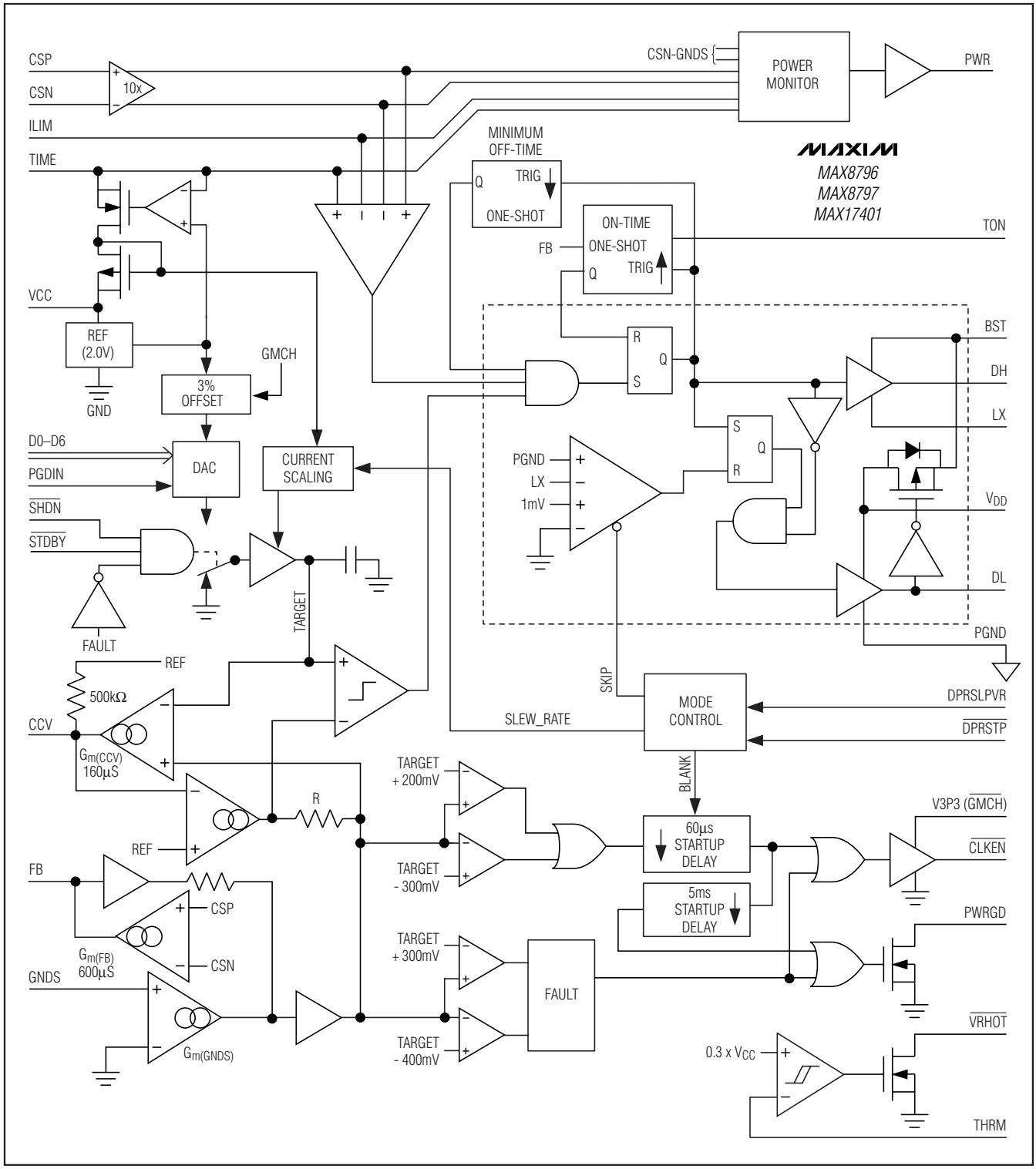



*Figure 3. Functional Diagram*

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

### +5V Bias Supply ($V_{CC}$ and $V_{DD}$)

The Quick-PWM controller requires an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95%-efficient, +5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the +5V bias supply can be generated with an external linear regulator.

The +5V bias supply must provide $V_{CC}$ (PWM controller) and $V_{DD}$ (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW}\left(Q_{G(LOW)} + Q_{G(HIGH)}\right)$$

where $I_{CC}$ is provided in the *Electrical Characteristics* table, $f_{SW}$ is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at $V_{GS}$ = 5V.

$V_{IN}$ and $V_{DD}$ can be connected if the input power source is a fixed +4.5V to +5.5V supply. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

### Switching Frequency (TON)

Connect a resistor ($R_{TON}$) between TON and $V_{IN}$ to set the switching period ($t_{SW} = 1/f_{SW}$):

$$t_{SW} = 16.3pF \times (R_{TON} + 6.5k\Omega)$$

A 96.75kΩ to 303.25kΩ corresponds to switching periods of 1.67µs (600kHz) to 5µs (200kHz), respectively. High-frequency (over 500kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (under 300kHz) operation offers the best overall efficiency at the expense of component size and board space.

### TON Open-Circuit Fault Protection

The TON input includes open-circuit protection to avoid long, uncontrolled on-times that could result in an overvoltage condition on the output. The MAX8796/MAX8797/MAX17401 detect an open-circuit fault if the TON current drops below 10µA for any reason—the TON resistor ($R_{TON}$) is unpopulated, a high resistance value is used, the input voltage is low, etc. Under these conditions, the MAX8796/MAX8797/MAX17401 stop switching (DH and DL pulled low) and immediately set the fault latch. Toggle $\overline{SHDN}$ or cycle the $V_{CC}$ power supply below 0.5V to clear the fault latch and reactivate the controller.

### On-Time One-Shot

The core contains a fast, low-jitter, adjustable one-shot that sets the high-side MOSFET's on-time. The one-shot varies the on-time in response to the input and feedback voltages. The main high-side switch on-time is inversely proportional to the input voltage as measured by the $R_{TON}$ input, and proportional to the feedback voltage ($V_{FB}$):

$$t_{ON} = t_{SW}\left(\frac{V_{FB}}{V_{IN}}\right)$$

where the switching period ($t_{SW} = 1/f_{SW}$) is set by the resistor between $V_{IN}$ and TON.

This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The on-time one-shots have good accuracy at the operating points specified in the *Electrical Characteristics* table. On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* table can vary over a wider range.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* table are influenced by switching delays in the external high-side MOSFET. Resistive losses, including the inductor, both MOSFETs, and printed-circuit board (PCB) copper losses in the output and ground tend to raise the switching frequency as the load current increases. Under light-load conditions, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only during forced-PWM operation and dynamic output-voltage transitions when the inductor current reverses at light- or negative-load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH-rising dead time. For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency is:

$$f_{SW} = \frac{(V_{OUT} + V_{DIS})}{t_{ON}(V_{IN} + V_{DIS} - V_{CHG})}$$

where $V_{DIS}$ is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances; $V_{CHG}$ is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PCB resistances; and $t_{ON}$ is the on-time as determined above.

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller



### Current Sense

The output current is differentially sensed by the high-impedance current-sense inputs (CSP and CSN). Low-offset amplifiers are used for voltage-positioning gain, current-limit protection, and power monitoring. Sensing the current at the output offers advantages, including less noise sensitivity and the flexibility to use either a current-sense resistor or the DC resistance of the power inductor.

Using the DC resistance ($R_{DCR}$) of the inductor allows higher efficiency. In this configuration, the initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and power monitor. This current-sense method uses an RC filtering network to extract the current information from the inductor (see Figure 4). The resistive divider used should provide a current-sense resistance ($R_{CS}$) low enough to meet the current-limit requirements ($R_{CS} \times I_{OUT(MAX)} < 50mV$), and the time constant of the RC network should match the inductor's time constant ($L/R_{DCR}$):

$$R_{CS} = \left(\frac{R2}{R1 + R2}\right) R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}} \left[\frac{1}{1} \quad \frac{1}{R2}\right]$$

where $R_{CS}$ is the required current-sense resistance, and $R_{DCR}$ is the inductor's series DC resistance. Use the worst-case inductance and $R_{DCR}$ values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load. To minimize the current-sense error due to the current-sense inputs' bias current ($I_{CSP}$), choose R1 ll R2 to be less than 2kΩ and use the above equation to determine the sense capacitance ($C_{EQ}$). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Voltage Positioning and Loop Compensation* section for detailed information.

When using a current-sense resistor for accurate output-voltage positioning, the circuit requires a differential RC filter to eliminate the AC voltage step caused by the equivalent series inductance ($L_{ESL}$) of the current-sense resistor (see Figure 4). The ESL-induced voltage step does not affect the average current-sense voltage, but results in a significant peak current-sense voltage error

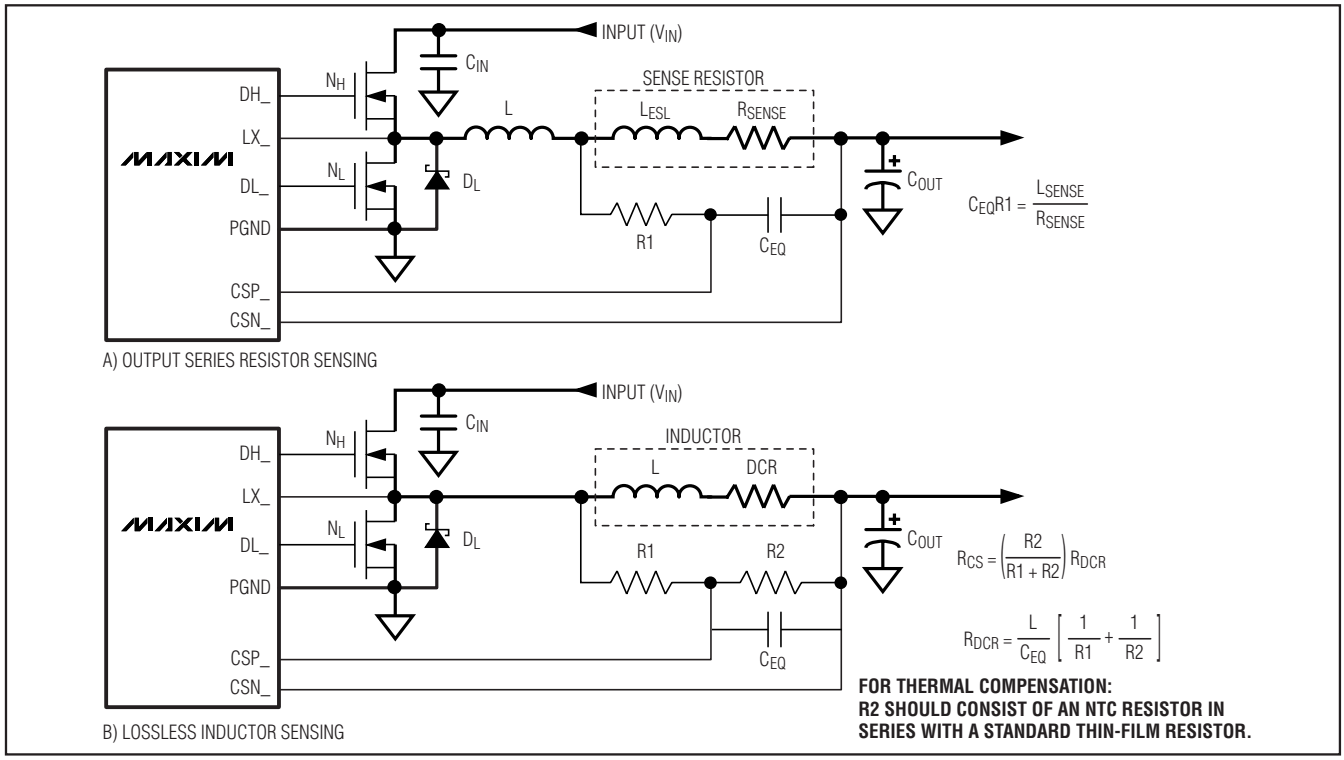



*Figure 4. Current-Sense Methods*

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

that results in unwanted offsets in the regulation voltage and results in early current-limit detection. Similar to the inductor DCR sensing method, the RC filter's time constant should match the L/R time constant formed by the current-sense resistor's parasitic inductance:

$$\frac{L_{ESL}}{R_{SENSE}} = C_{EQ}R1$$

where $L_{ESL}$ is the equivalent series inductance of the current-sense resistor, $R_{SENSE}$ is the current-sense resistance value, $C_{EQ}$ and R1 are the time-constant matching components.

### Current Limit

The current-limit circuit employs a "valley" current-sensing algorithm that uses a current-sense element (see Figure 4) between the current-sense inputs (CSP to CSN) to detect the inductor current. If the differential current-sense voltage exceeds the current-limit threshold, the PWM controller does not initiate a new cycle until the inductor current drops below the valley current-limit threshold. Since only the valley current level is actively limited, the actual peak inductor current exceeds the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense impedance, inductor value, and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

The positive valley current-limit threshold voltage at CSP to CSN equals precisely 1/10 of the differential TIME to ILIM voltage over a 0.1V to 0.5V range (10mV to 50mV current-sense range). Connect ILIM directly to $V_{CC}$ to set the default current-limit threshold setting of 22.5mV nominal for IMVP-6 (MAX8796/MAX17401: V3P3 = 3.3V) and 17.5mV nominal for GMCH (MAX8797 and MAX8796/MAX17401: V3P3 = GND).

The negative current-limit threshold (forced-PWM mode only) is nominally -125% of the corresponding valley current-limit threshold. When the inductor current drops below the negative current limit, the controller immediately activates an on-time pulse—DL turns off, and DH turns on—allowing the inductor current to remain above the negative current threshold.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by the current-sense inputs (CSP, CSN).

### Feedback

The nominal no-load output voltage ($V_{TARGET}$) is defined by the VID-selected DAC voltage (see Tables 3 and 4) plus the remote ground-sense adjustment ($V_{GNDS}$) as defined in the following equation:

$$V_{TARGET} = V_{FB} = V_{DAC} + V_{GNDS}$$

where $V_{DAC}$ is the selected VID voltage. On startup, IMVP-6 (MAX8796/MAX17401: V3P3 = 3.3V) applications slew the target voltage from ground to the preset boot voltage and GMCH (MAX8797 or MAX8796/MAX17401: V3P3 = GND) applications slew the target voltage directly to the VID-selected DAC target.

### Voltage-Positioning Amplifier (Steady-State Droop)

The MAX8796/MAX8797/MAX17401 include a transconductance amplifier for adding gain to the voltage-positioning sense path. The amplifier's input is generated by the differential current-sense inputs, which sense the inductor current by measuring the voltage across either current-sense resistors or the inductor's DCR. The amplifier's output connects directly to the regulator's voltage-positioned feedback input (FB), so the resistance between FB and the output-voltage sense point determines the voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{FB}I_{FB}$$

where the target voltage ($V_{TARGET} = V_{FB}$) is defined by the selected VID code (Table 3 for IMVP6 or Table 4 for GMCH), and the FB amplifier's output current ($I_{FB}$) is determined by the sum of the current-sense voltages:

$$I_{FB} = G_{m(FB)}(V_{CSP} - V_{CSN})$$

where $G_{m(FB)}$ is typically 600µS as defined in the *Electrical Characteristics* table.

### Differential Remote Sense

The MAX8796/MAX8797/MAX17401 include differential, remote-sense inputs to eliminate the effects of voltage drops along the PCB traces and through the processor's power pins. The feedback-sense node connects to the voltage-positioning resistor ($R_{FB}$). The ground-sense (GNDS) input connects to an amplifier that adds an offset directly to the feedback voltage, effectively adjusting the output voltage to counteract the voltage drop in the ground path. Connect the voltage-positioning resistor ($R_{FB}$) and ground-sense (GNDS) input directly to the processor's remote-sense outputs as shown in Figures 1 and 2.

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller



### Integrator Amplifier

An integrator amplifier forces the DC average of the FB voltage to equal the target voltage. This transconductance amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 3), allowing accurate DC output-voltage regulation regardless of the output ripple voltage. The integrator amplifier has the ability to shift the output voltage by ±50mV (typ). The integration time constant can be set easily with an external compensation capacitor between CCV and analog ground, with the minimum recommended CCV capacitor value determined by:

$$C_{CCV} >> G_{m(CCV)}/(16\pi \times f_{SW})$$

where $G_{m(CCV)}$ = 320µS (max) is the integrator's transconductance and $f_{SW}$ is the switching frequency set by the $R_{TON}$ resistance.

The MAX8796/MAX8797/MAX17401 disable the integrator by connecting the amplifier inputs together at the beginning of all downward VID transitions done in pulse-skipping mode (DPRSLPVR = high). The integrator remains disabled until 20µs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

### DAC Inputs (D0–D6)

The digital-to-analog converter (DAC) programs the output voltage using the D0–D6 inputs. D0–D6 are low-voltage (1.0V) logic inputs designed to interface directly with the CPU. Do not leave D0–D6 unconnected. Changing D0–D6 initiates a transition to a new output-voltage level. Change D0–D6 together, avoiding greater than 20ns skew between bits. Otherwise, incorrect DAC readings can cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages are compatible with the Intel IMVP-6 (Table 3) and Intel GMCH specifications (Table 4).

**Table 3. IMVP-6 Output Voltage VID DAC Codes (MAX8796/MAX17401 V3P3 = 3.3V)**

| D6 | D5 | D4 | D3 | D2 | D1 | D0 | IMVP-6 OUTPUT VOLTAGE (V) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.5000 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1.4875 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.4750 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1.4625 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.4500 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.4375 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.4250 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.4125 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1.4000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.3875 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1.3750 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1.3625 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.3500 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1.3375 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1.3250 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.3125 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1.3000 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1.2875 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1.2750 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1.2625 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1.2500 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0.7000 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0.6875 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0.6750 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0.6625 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0.6500 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0.6375 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0.6250 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0.6125 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0.6000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0.5875 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0.5750 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0.5625 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0.5500 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0.5375 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0.5250 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0.5125 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0.5000 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0.4875 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0.4750 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0.4625 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0.4500 |

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

**Table 3. IMVP-6 Output Voltage VID DAC Codes (MAX8796/MAX17401 V3P3 = 3.3V) (continued)**

| D6 | D5 | D4 | D3 | D2 | D1 | D0 | IMVP-6 OUTPUT VOLTAGE (V) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1.2375 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1.2250 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1.2125 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1.2000 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1.1875 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1.1750 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1.1625 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1.1500 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1.1375 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1.1250 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1.1125 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1.1000 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1.0875 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1.0750 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1.0625 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1.0500 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1.0375 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1.0250 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1.0125 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1.0000 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0.9875 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0.9750 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0.9625 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0.9500 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0.9375 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0.9250 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0.9125 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0.9000 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0.8875 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0.8750 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0.8625 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0.8500 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0.8375 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0.8250 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0.8125 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0.8000 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0.7875 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0.7750 |

| D6 | D5 | D4 | D3 | D2 | D1 | D0 | IMVP-6 OUTPUT VOLTAGE (V) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0.4375 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0.4250 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0.4125 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0.4000 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0.3875 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0.3750 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0.3625 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0.3500 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0.3375 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0.3250 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0.3125 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0.3000 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0.2875 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0.2750 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0.2625 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0.2500 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0.2375 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0.2250 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0.2125 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0.2000 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0.1875 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0.1750 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0.1625 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0.1500 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0.1375 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0.1250 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0.1125 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0.1000 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0.0875 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0.0750 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0.0625 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0.0500 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0.0375 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0.0250 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0.0125 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

**Table 3. IMVP-6 Output Voltage VID DAC Codes (MAX8796/MAX17401 V3P3 = 3.3V) (continued)**

| D6 | D5 | D4 | D3 | D2 | D1 | D0 | IMVP-6 OUTPUT VOLTAGE (V) |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0.7625 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0.7500 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0.7375 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0.7250 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0.7125 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

**Table 4. GMCH Output Voltage VID DAC Codes (MAX8797 or MAX8796/MAX17401 when V3P3 = GND)**

| D4 | D3 | D2 | D1 | D0 | GMCH OUTPUT VOLTAGE (V) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1.28750 |
| 0 | 0 | 0 | 0 | 1 | 1.26175 |
| 0 | 0 | 0 | 1 | 0 | 1.23600 |
| 0 | 0 | 0 | 1 | 1 | 1.21025 |
| 0 | 0 | 1 | 0 | 0 | 1.18450 |
| 0 | 0 | 1 | 0 | 1 | 1.15875 |
| 0 | 0 | 1 | 1 | 0 | 1.13300 |
| 0 | 0 | 1 | 1 | 1 | 1.10725 |
| 0 | 1 | 0 | 0 | 0 | 1.08150 |
| 0 | 1 | 0 | 0 | 1 | 1.05575 |
| 0 | 1 | 0 | 1 | 0 | 1.03000 |
| 0 | 1 | 0 | 1 | 1 | 1.00425 |
| 0 | 1 | 1 | 0 | 0 | 0.97850 |
| 0 | 1 | 1 | 0 | 1 | 0.95275 |
| 0 | 1 | 1 | 1 | 0 | 0.92700 |
| 0 | 1 | 1 | 1 | 1 | 0.90125 |
| 1 | 0 | 0 | 0 | 0 | 0.87750 |
| 1 | 0 | 0 | 0 | 1 | 0.84975 |
| 1 | 0 | 0 | 1 | 0 | 0.82400 |
| 1 | 0 | 0 | 1 | 1 | 0.79825 |
| 1 | 0 | 1 | 0 | 0 | 0.77250 |
| 1 | 0 | 1 | 0 | 1 | 0.74675 |
| 1 | 0 | 1 | 1 | 0 | 0.72100 |
| 1 | 0 | 1 | 1 | 1 | 0.69525 |
| 1 | 1 | 0 | 0 | 0 | 0.66950 |
| 1 | 1 | 0 | 0 | 1 | 0.64375 |
| 1 | 1 | 0 | 1 | 0 | 0.61800 |
| 1 | 1 | 0 | 1 | 1 | 0.59225 |
| 1 | 1 | 1 | 0 | 0 | 0.56650 |
| 1 | 1 | 1 | 0 | 1 | 0.54075 |
| 1 | 1 | 1 | 1 | 0 | 0.51500 |
| 1 | 1 | 1 | 1 | 1 | 0.41200 |

### *Output-Voltage Transition Timing*

The MAX8796/MAX8797/MAX17401 perform mode transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly ideal transitions, guaranteeing just-in-time arrival at the new output voltage level with the lowest possible peak currents for a given output capacitance.

At the beginning of an output-voltage transition, the MAX8796/MAX8797/MAX17401 blank both PWRGD thresholds, preventing the PWRGD open-drain output and the $\overline{CLKEN}$ push-pull output from changing states during the transition. The controller reenables the lower PWRGD threshold approximately 20µs after the slew-rate controller reaches the target output voltage. The controller reenables the upper PWRGD threshold 20µs after the slew-rate controller reaches the target output voltage only for upward VID transitions. For downward VID transitions, the MAX8796/MAX8797/MAX17401 must also detect an error amplifier transition (feedback drops below the new target threshold) before reenabling the upper PWRGD transition to avoid false PWRGD errors under pulse-skipping conditions. The slew rate (set by resistor $R_{TIME}$) must be set fast enough to ensure that the transition can be completed within the maximum allotted time.

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

The MAX8796/MAX8797/MAX17401 automatically control the current to the minimum level required to complete the transition in the calculated time. The slew-rate controller uses an internal capacitor and current-source programmed by $R_{TIME}$ to transition the output voltage. The total transition time depends on $R_{TIME}$, the voltage difference, and the accuracy of the slew-rate controller ($C_{SLEW}$ accuracy). The slew rate is not dependent on the total output capacitance, as long as the surge current is less than the current limit. For all dynamic VID transitions, the transition time ($t_{TRAN}$) is given by:

$$t_{TRAN} = \frac{|V_{NEW} - V_{OLD}|}{(dV_{TARGET}/dt)}$$

where $dV_{TARGET}/dt$ = 12.5mV/µs x 71.5kΩ/$R_{TIME}$ is the slew rate, $V_{OLD}$ is the original output voltage, and $V_{NEW}$ is the new target voltage. See TIME Slew-Rate Accuracy in the *Electrical Characteristics* table for slew-rate limits. For soft-start and shutdown, the controller automatically reduces the slew rate to 1/8.

The output voltage tracks the slewed target voltage, making the transitions relatively smooth. Excluding the load current, the average inductor current required to make an output voltage transition is:

$$I_L \cong C_{OUT} \times (dV_{TARGET}/dt)$$

where $dV_{TARGET}/dt$ is the required slew rate and $C_{OUT}$ is the total output capacitance.

### *IMVP-6 Deeper Sleep Transitions*

When DPRSLPVR goes high, the MAX8796/MAX17401 immediately enter pulse-skipping operation (see Figures 5, 6, 7). If the VIDs are set to a lower voltage setting, the output drops at a rate determined by the load and the output capacitance. The internal target still ramps as before, and the upper PWRGD threshold remains blanked high impedance until the output voltage reaches the internal target:

- **Fast C4E deeper sleep exit:** When exiting deeper sleep (DPRSLPVR pulled low) while the output voltage still exceeds the deeper sleep voltage, the MAX8796/MAX17401 quickly slew (50mV/µs min regardless of $R_{TIME}$ setting) the internal target voltage to the DAC code provided by the processor as long as the output voltage is above the new target. The controller remains in skip mode until the output voltage equals the internal target (until the first on-time is triggered by the error amplifier). Once the internal target reaches the output voltage, switching begins and the controller is allowed to enter forced-PWM mode. The controller blanks PWRGD and $\overline{CLKEN}$ (forced high impedance) until 20µs after the transition is completed. See Figure 5.

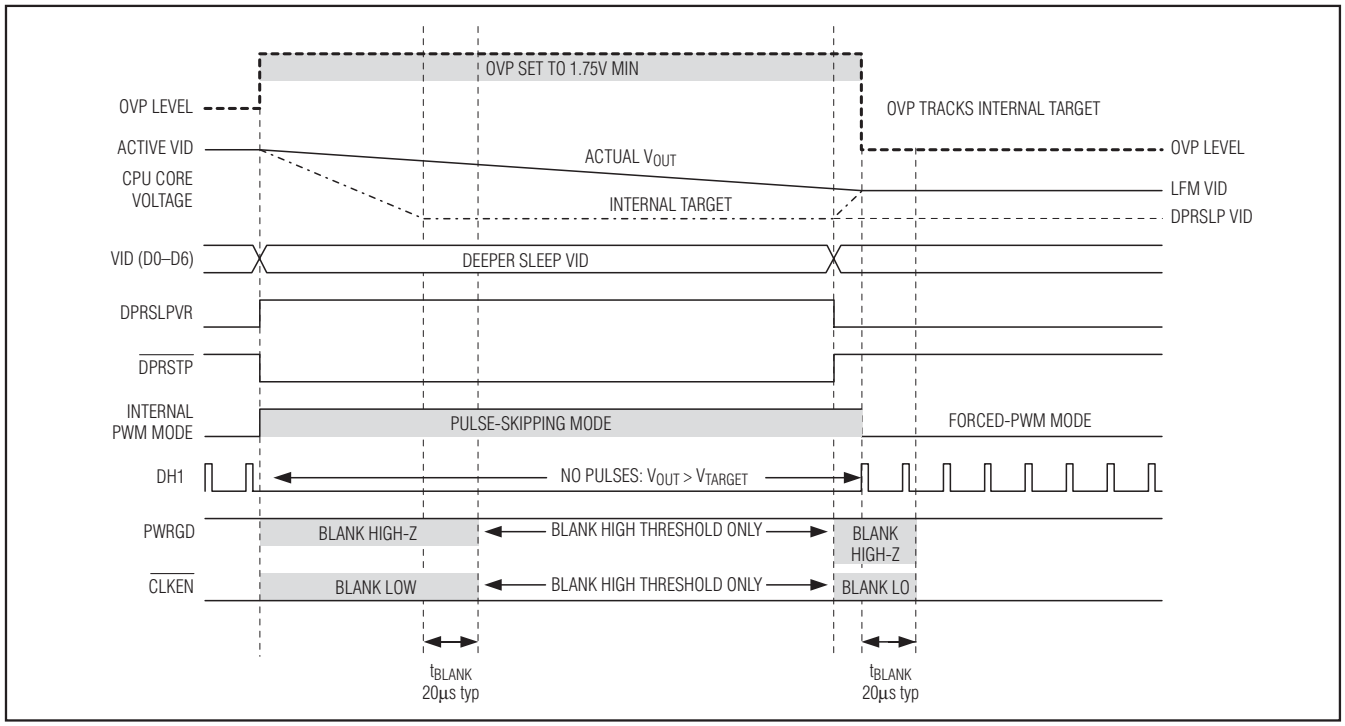



*Figure 5. IMVP-6 C4E (C4 Early Exit) Transition*

- **Standard C4 deeper sleep exit:** When exiting deeper sleep (DPRSLPVR pulled low) while the output voltage is regulating to the deeper sleep voltage, the MAX8796/MAX17401 immediately ramp the output voltage to the LFM DAC code provided by the processor at the slew rate set by $R_{TIME}$. The controller blanks PWRGD and $\overline{CLKEN}$ (forced high impedance) until 20µs after the transition is completed. See Figure 6.

- **Slow C4 deeper sleep exit:** When exiting deeper sleep (DPRSLPVR stays high, $\overline{DPRSTP}$ pulled high) while the output voltage is regulating to the deeper sleep voltage, the MAX8796/MAX17401 remain in skip mode and ramp the output voltage to the LFM DAC code provided by the processor at 1/4 the slew rate set by $R_{TIME}$. The controller blanks PWRGD and $\overline{CLKEN}$ (forced high impedance) until 20µs after the transition is completed. See Figure 7.

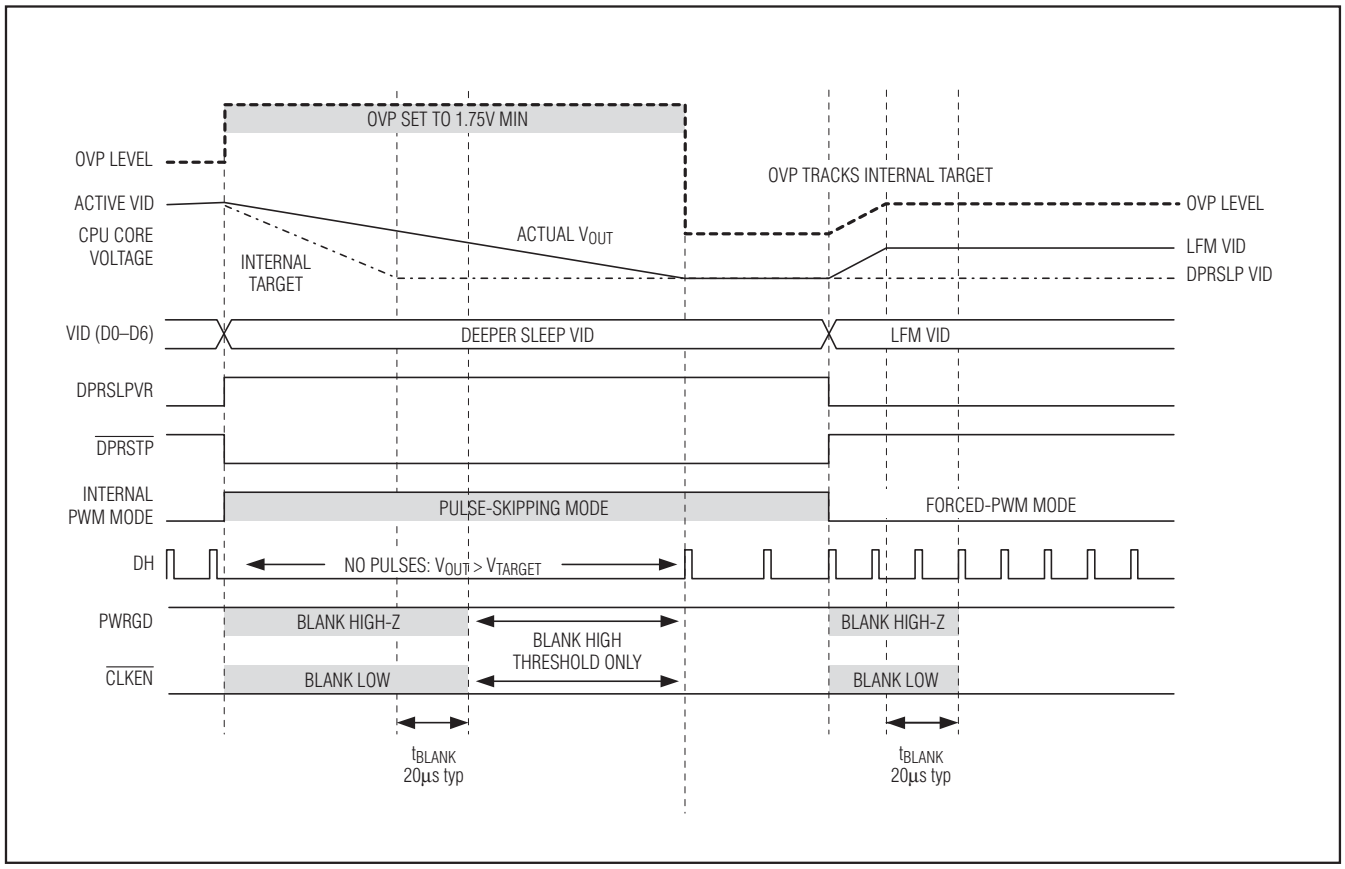



*Figure 6. Standard IMVP-6 C4 Transition*

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

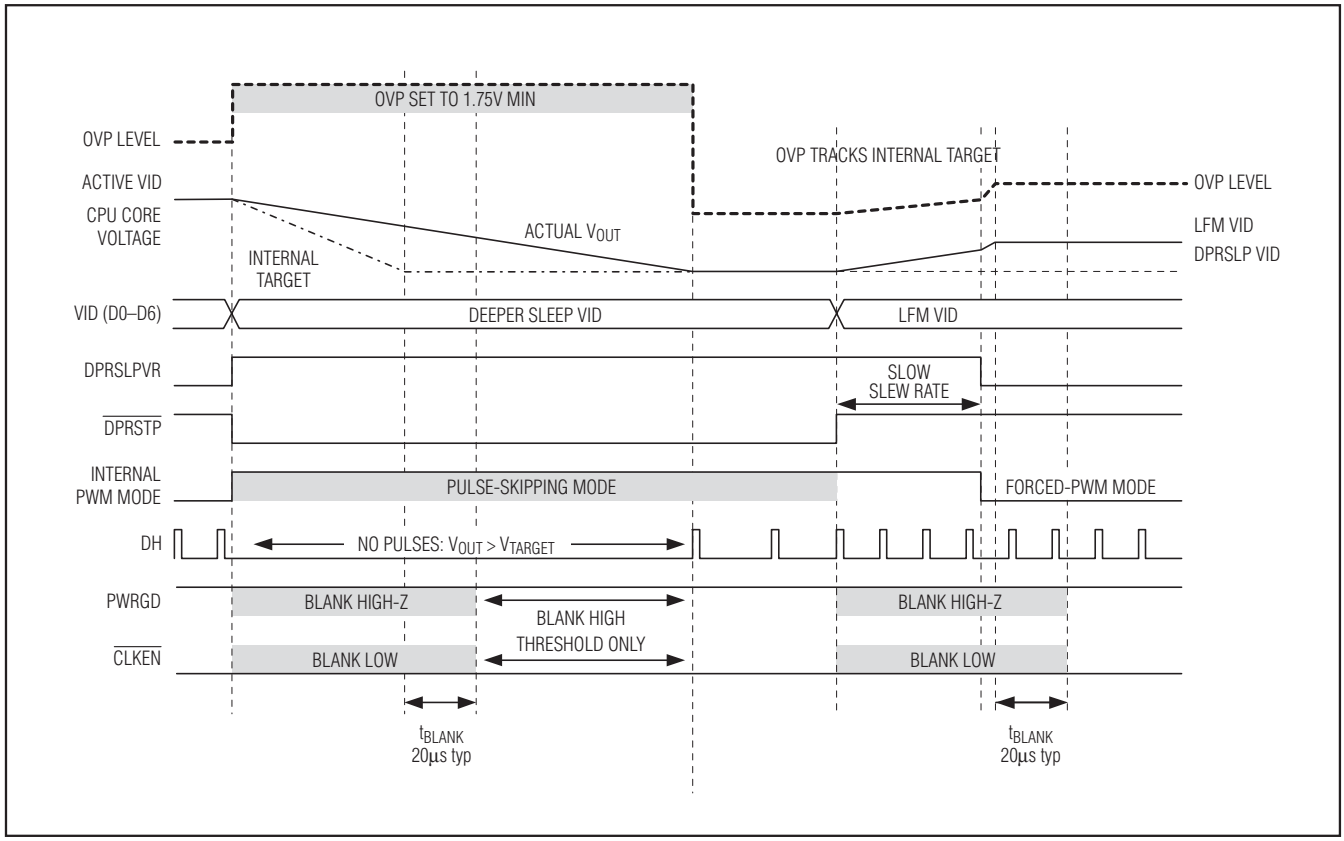



*Figure 7. IMVP-6 Slow C4 Transition*

### *GMCH Sleep Transition*

For GMCH applications—the MAX8796/MAX17401 (V3P3 = GND) or MAX8797—the system enters the sleep state by selecting a lower VID DAC code. When DPRSLPVR is forced high (for the best light-load efficiency), the controller operates in a pulse-skipping mode and passively transitions to the lower sleep voltage. Once the VIDs are set to a lower voltage setting, the output drops at a rate determined by the load and the output capacitance while the internal target ramps down at the slew rate set by R TIME. The upper PWRGD threshold remains blanked high impedance until the output voltage reaches the internal target:

- **Standard GMCH sleep exit:** When exiting the sleep state while the output voltage is regulating to the selected sleep VID voltage, the controller immediately ramps the output voltage to the newly selected active VID code at the slew rate set by $R_{TIME}$. The controller blanks PWRGD (forced high impedance) until 20µs after the transition is completed. See Figure 8.
- **Early GMCH sleep exit:** When exiting the sleep state while the output voltage still exceeds the internal target (the sleep voltage), the controller quickly slews (50mV/µs min regardless of R TIME setting) the internal target voltage to the new VID DAC code as long as the output voltage exceeds the new target. Once the internal target reaches the output voltage, switching begins and the controller continues to ramp up the internal target and output voltage at the slew rate selected by R TIME. The controller blanks PWRGD (forced high impedance) until 20µs after the transition is completed. See Figure 9.

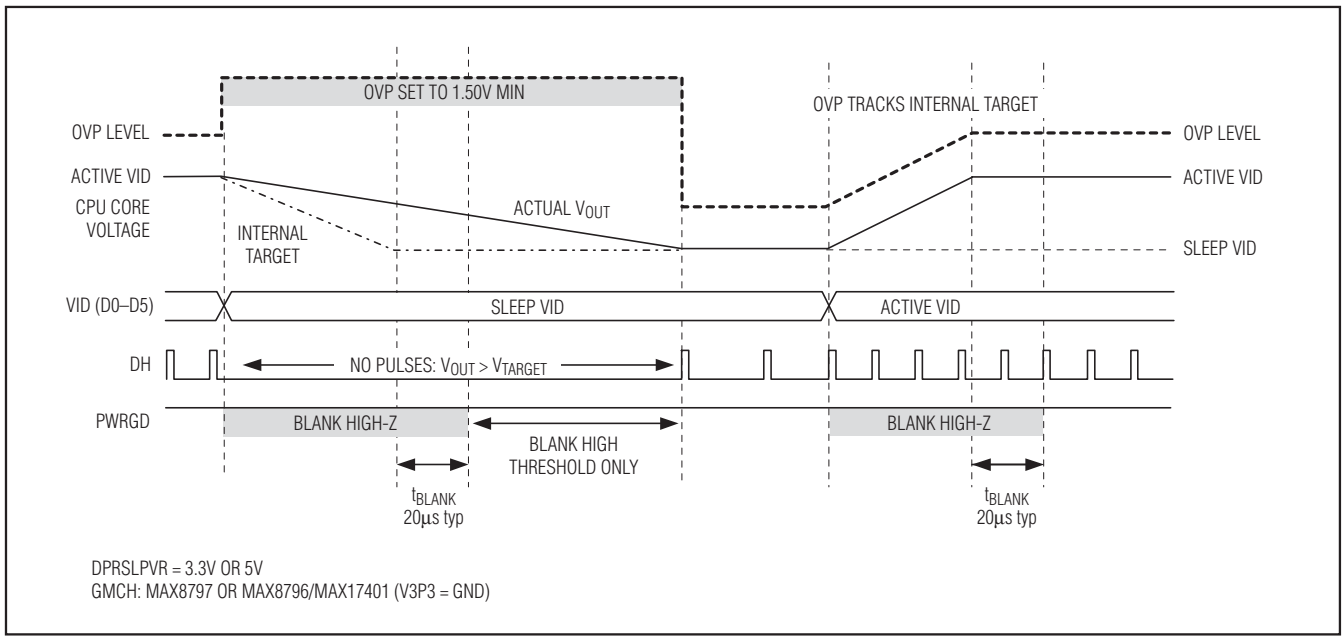



*Figure 8. Standard GMCH Sleep Transition*

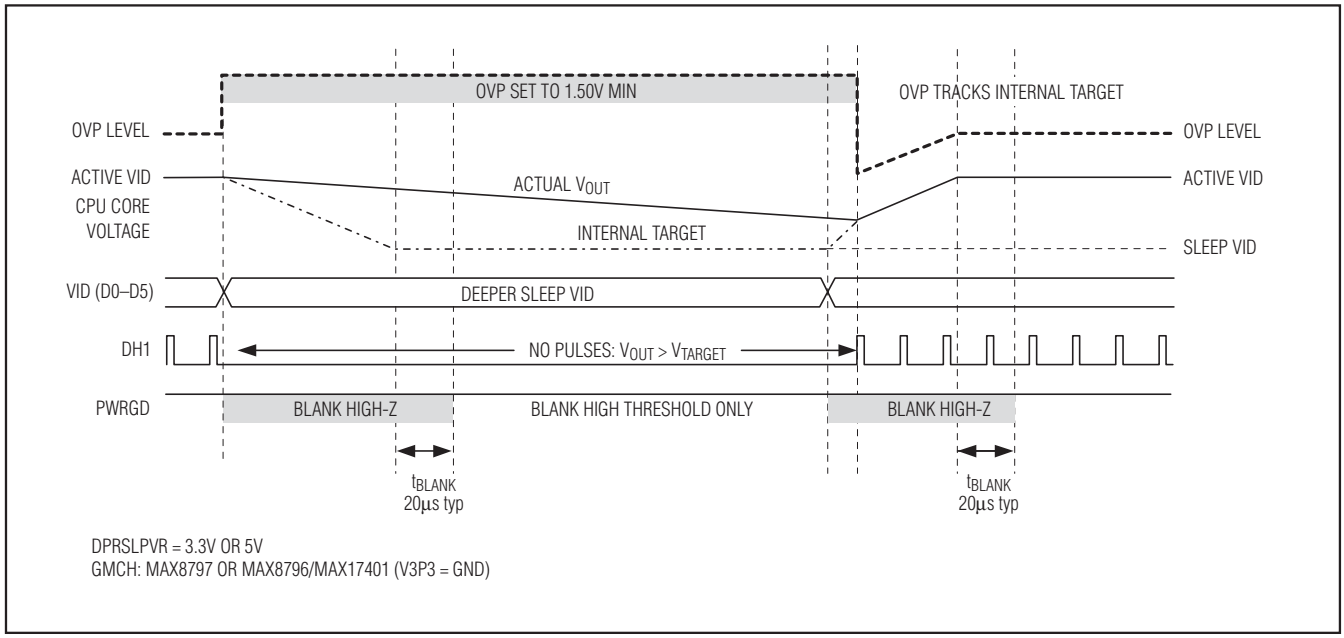



*Figure 9. Early Exit GMCH Sleep Transition*

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

### Forced-PWM Operation (Normal Mode)

During soft-shutdown and normal operation—when the CPU is actively running (DPRSLPVR = low, Table 5)—the MAX8796/MAX8797/MAX17401 operate with the low-noise, forced-PWM control scheme. Forced-PWM operation disables the zero-crossing comparator, forcing the low-side gate-drive waveforms to constantly be the complement of the high-side gate-drive waveforms. This keeps the switching frequency constant and allows the inductor current to reverse under light loads, providing fast, accurate negative output-voltage transitions by quickly discharging the output capacitors.

Forced-PWM operation comes at a cost: the no-load +5V bias supply current remains between 10mA to 50mA, depending on the external MOSFETs and switching frequency. To maintain high efficiency under light-load conditions, the processor can switch the controller to a low-power pulse-skipping control scheme after entering suspend mode. The MAX8796/MAX8797/MAX17401 automatically use pulse-skipping operation during soft-start, regardless of the DPRSLPVR configuration.

### Light-Load Pulse-Skipping Operation (Deeper Sleep)

During soft-start and sleep states—DPRSLPVR is pulled high—the MAX8796/MAX8797/MAX17401 operate in pulse-skipping mode. The pulse-skipping mode enables the driver's zero-crossing comparator, so the controller pulls DL low when the low-side MOSFET voltage drop (LX to GND voltage) detects "zero" inductor current. This keeps the inductor from sinking current and discharging the output capacitors and forces the controller to skip pulses under light-load conditions to avoid overcharging the output.

Upon entering pulse-skipping operation, the controller temporarily blanks the upper PWRGD and $\overline{CLKEN}$ thresholds, and sets the transitional OVP threshold to 300mV above the maximum VID voltage allowed—1.80V for IMVP-6 and 1.55V for GMCH—to prevent false OVP faults when the transition to pulse-skipping operation coincides with a VID code change. Once the error amplifier detects that the output voltage is in regulation, the upper PWRGD, upper $\overline{CLKEN}$, and OVP thresholds resume tracking the selected VID DAC code. The MAX8796/MAX8797/MAX17401 automatically use forced-PWM operation during soft-shutdown, regardless of the DPRSLPVR configuration.

### Automatic Pulse-Skipping Switchover

In skip mode (DPRSLPVR = high), an inherent automatic switchover to PFM takes place at light loads (Figure 10). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current across the low-side MOSFETs. Once $V_{LX}$ drops below the zero-crossing comparator threshold (see the *Electrical Characteristics* table), the comparator forces DL low (Figure 3). This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The PFM/PWM crossover occurs when the load-current is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 10). For a battery input range of 7V to 20V, this threshold is relatively constant, with only a minor dependence on the input voltage due to the typically low duty cycles. The total load current at the PFM/PWM crossover threshold ($I_{LOAD(SKIP)}$) is approximately:

$$I_{LOAD(SKIP)} = \left(\frac{t_{SW} V_{OUT}}{L}\right)\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The switching waveforms might appear noisy and asynchronous when light loading activates pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs between PFM noise and light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response, especially at low input-voltage levels.

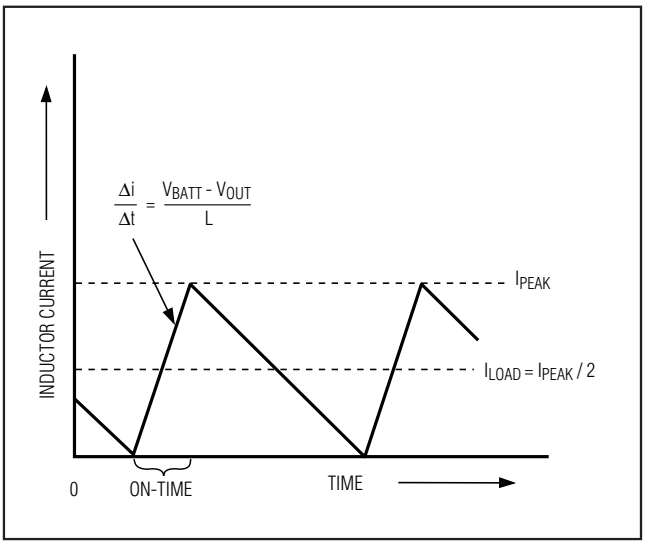



*Figure 10. Pulse-Skipping/Discontinuous Crossover Point*

**Table 5. Operating Mode Truth Table**

| $\overline{SHDN}$ | $\overline{DPRSTP}$ (IMVP-6 ONLY) | DPRSLPVR | OPERATING MODE | |
|---|---|---|---|---|
| GND | X | X | DISABLED | LOW-POWER SHUTDOWN. DL forced low, and the controller is disabled. The supply current drops below 3µA (1µA max per supply pin). |
| Rising X | | X | Pulse skipping 1/8 $R_{TIME}$ slew rate | STARTUP: When $\overline{SHDN}$ is pulled high, the MAX8796/MAX8797/MAX17401 begin the startup sequence after the internal circuitry powers up. The MAX8796/MAX8797/MAX17401 enable the PWM controller and ramp the output voltage up to the startup voltage. See Figures 11 and 12. |
| High X | | Low | Forced-PWM nominal $R_{TIME}$ slew rate | FULL POWER: The no-load output voltage is determined by the selected VID DAC code (Tables 3 and 4). |
| High L | ow | High | Pulse-skipping nominal $R_{TIME}$ slew rate | DEEPER SLEEP MODE: The no-load output voltage is determined by the selected VID DAC code (Tables 3 and 4). When DPRSLPVR is pulled high, the controller immediately enters 1-phase pulse-skipping operation, allowing automatic PWM/PFM switchover under light loads. The PWRGD and $\overline{CLKEN}$ upper thresholds are blanked during the transition. |
| High Hi | gh | High | Pulse-skipping 1/4 $R_{TIME}$ slew rate | DEEPER SLEEP SLOW EXIT MODE (IMVP-6 ONLY). The no-load output voltage is determined by the selected VID DAC code (Table 3). When $\overline{DPRSTP}$ is pulled high while DPRSLPVR is already high, the MAX8796/MAX17401 remains in pulse-skipping operation, allowing automatic PWM/PFM switchover under light loads. The PWRGD and $\overline{CLKEN}$ thresholds are blanked during the transition. |
| Falling X | | X | Forced-PWM 1/8 $R_{TIME}$ slew rate | SHUTDOWN. When $\overline{SHDN}$ is pulled low, the MAX8796/MAX8797/MAX17401 immediately pull PWRGD low, $\overline{CLKEN}$ becomes high impedance, and the output voltage is ramped down to ground. Once the output reaches zero, the controller enters the low-power shutdown state. See Figures 11 and 12. |
| High | X | X | DISABLED | FAULT MODE. The fault latch has been set by the MAX8796/MAX8797/MAX17401 UVP fault, $R_{TON}$ open fault, or thermal-shutdown protection and MAX8796/MAX8797 OVP fault. The controller remains in FAULT mode until $V_{CC}$ power is cycled or $\overline{SHDN}$ toggled. |

### *Power-Up Sequence (POR, UVLO)*

The MAX8796/MAX8797/MAX17401 are enabled when $\overline{SHDN}$ is driven high (Figures 11 and 12). The internal reference powers up first, followed by the analog control circuitry. Roughly 50µs after the analog control circuitry powers up, the PWM controller is enabled and begins the soft-start sequence.

Power-on reset (POR) occurs when $V_{CC}$ rises above approximately 2V, resetting the fault latch and preparing the controller for operation. The $V_{CC}$ UVLO circuitry inhibits switching until $V_{CC}$ rises above 4.25V. The controller powers up the reference once the system enables the controller, $V_{CC}$ is above 4.25V, and $\overline{SHDN}$ is driven high. The soft-start sequence ramps the output voltage up to the target voltage—either the 1.20V boot voltage for IMVP-6 or the selected VID voltage for GMCH—at 1/8 the nominal slew rate set by $R_{TIME}$:

$$t_{TRAN(START)} = \frac{8V_{START}}{(dV_{TARGET}/dt)}$$

where $dV_{TARGET}/dt$ = 12.5mV/µs x 71.5k Ω/$R_{TIME}$ is the nominal slew rate. The soft-start circuitry does not use a variable current limit, so full output current is available immediately. The MAX8796/MAX8797/MAX17401 automatically use pulse-skipping mode during soft-start and use forced-PWM mode during soft-shutdown, regardless of the DPRSLPVR configuration.

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

For IMVP-6 applications (MAX8796/MAX17401 with V3P3 = 3.3V), the MAX8796/MAX17401 pull $\overline{CLKEN}$ low approximately 60µs after reaching the boot voltage. At the same time, the MAX8796/MAX17401 slew the output to the selected VID voltage at the programmed nominal slew rate. PWRGD becomes high impedance approximately 5ms after $\overline{CLKEN}$ is pulled low.

For GMCH applications (MAX8797 or MAX8796/MAX17401 with V3P3 = GND), PWRGD becomes high impedance approximately 60µs after reaching the selected VID voltage.

For automatic startup, the battery voltage should be present before $V_{CC}$ rises above its UVLO threshold.

If the controller attempts to bring the output into regulation without the battery voltage present, the output undervoltage fault latch disables the controller. The MAX8796/MAX8797/MAX17401 remain shut down until the fault latch is cleared by toggling $\overline{SHDN}$ or cycling the $V_{CC}$ power supply below 0.5V.

If the $V_{CC}$ voltage drops below 4.25V, the controller assumes that there is not enough supply voltage to make valid decisions. To protect the output from overvoltage faults, the controller shuts down immediately and forces a high-impedance output (DL and DH pulled low) and pulls CSN low through a 10Ω discharge MOSFET.

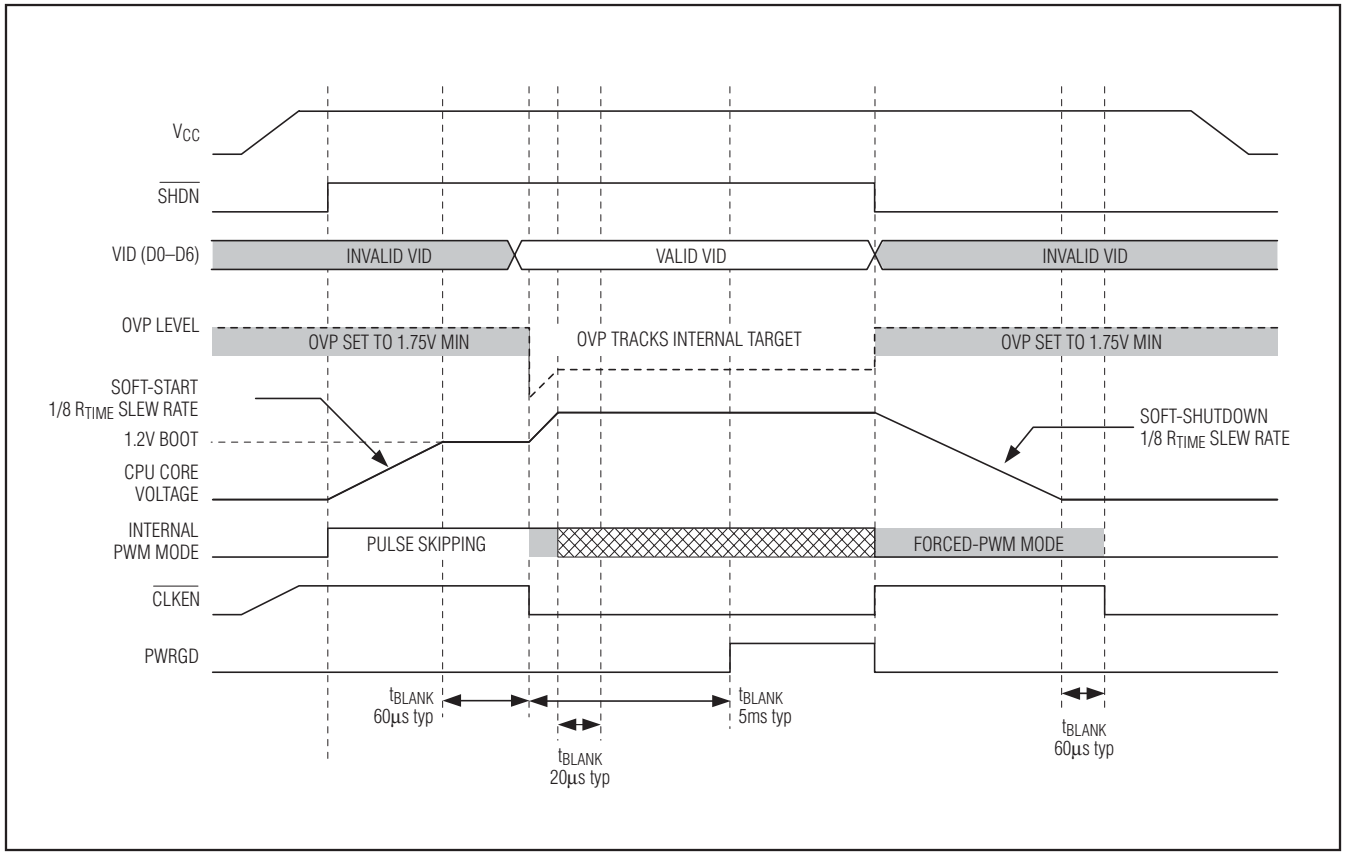



*Figure 11. IMVP-6 Power-Up and Shutdown Sequence Timing Diagram*

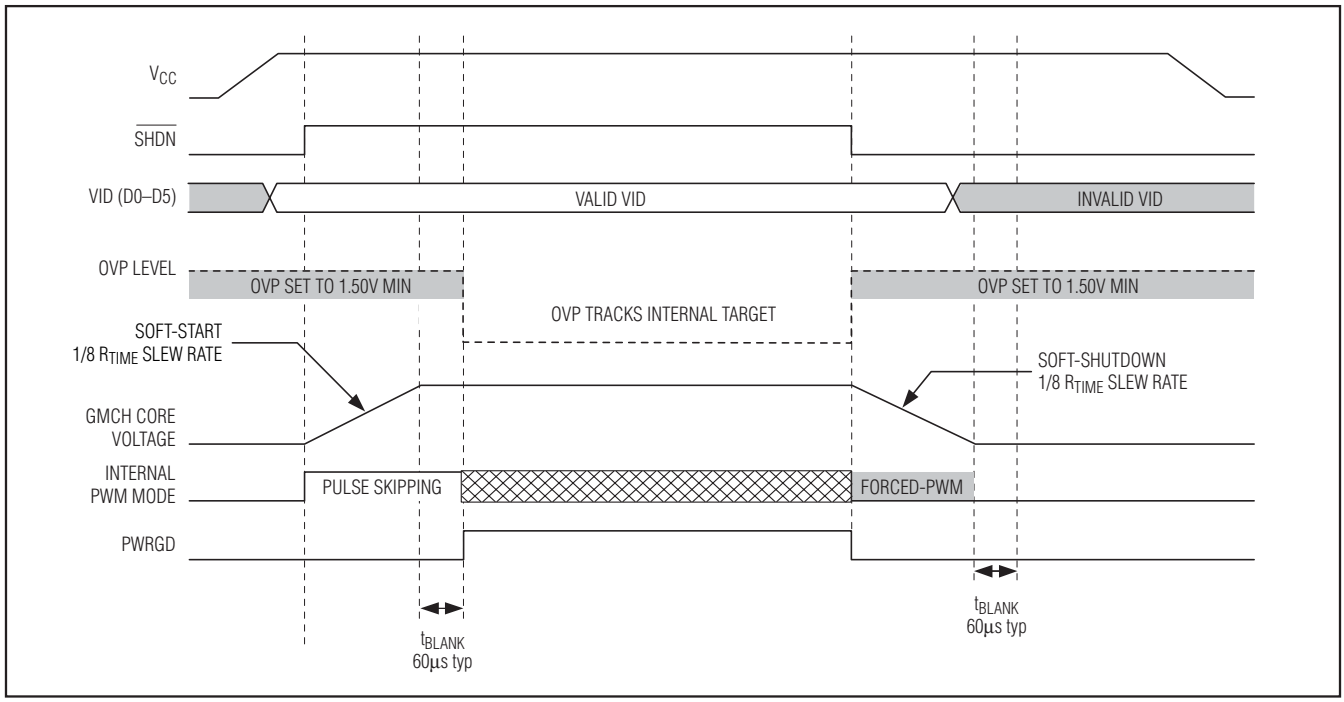



*Figure 12. GMCH Power-Up and Shutdown Sequence Timing Diagram*

### Shutdown

When $\overline{SHDN}$ goes low, the MAX8796 / MAX8797/ MAX17401 enter low-power shutdown mode. PWRGD is pulled low immediately, and the output voltage ramps down at 1/8 the slew rate set by $R_{TIME}$:

$$t_{TRAN(SHDN)} = \frac{8V_{OUT}}{(dV_{TARGET}/dt)}$$

where $dV_{TARGET}/dt$ = 12.5mV/µs x 71.5k Ω/$R_{TIME}$ is the nominal slew rate. Slowly discharging the output capacitors by slewing the output over a long period of time keeps the average negative inductor current low (damped response), thereby eliminating the negative output-voltage excursion that occurs when the controller discharges the output quickly by permanently turning on the low-side MOSFET (underdamped response). This eliminates the need for the Schottky diode connected between the output and ground to clamp the negative output-voltage excursion. After the controller reaches the zero target, the MAX8796/ MAX8797/MAX17401 shut down completely—the drivers are disabled (DL and DH are pulled low)—the internal reference turns off, and the supply currents drop to about 1µA (max).

When an output undervoltage fault condition activates the shutdown sequence, the protection circuitry sets the UVP fault latch to prevent the controller from restarting. To clear the fault latch and reactivate the controller, toggle $\overline{SHDN}$ or cycle $V_{CC}$ power below 0.5V.

### Power Monitor (PWR)

The MAX8796/MAX8797/MAX17401 include a single-quadrant multiplier used to determine the actual output power based on the inductor current (the differential CS input) and output voltage (CSN to GNDS). The buffered output of this multiplier is connected to PWR and provides a voltage relative to the output power dissipation:

$$V_{PWR} = \frac{K_{PWR}(V_{CSN} - V_{GNDS})(V_{CSP} - V_{CSN})}{(V_{TIME} - V_{ILIM})}$$

where $V_{CSP}$ - $V_{CSN}$ = $I_{LOAD}$ x $R_{SENSE}$, and the power-monitor scale factor ($K_{PWR}$) is typically 25. The power monitor allows the system to accurately monitor the CPU's power dissipation and quickly predict if the system is about to overheat before the significantly slower temperature sensor signals an overtemperature alert.

# 1-Phase Quick-PWM Intel IMVP-6/GMCH Controller

### Temperature Comparator (VRHOT)

The MAX8796/MAX8797/MAX17401 also feature an independent comparator with an accurate threshold that tracks the analog supply voltage ($V_{HOT}$ = 0.3 x $V_{CC}$). This makes the thermal trip threshold independent of the $V_{CC}$ supply voltage tolerance. Use a resistor- and thermistor-divider between $V_{CC}$ and GND to generate a voltage-regulator overtemperature monitor. Place the thermistor as close to the MOSFETs and inductors as possible.

### Fault Protection (Latched)

#### Output Overvoltage Protection (OVP) (MAX8796/MAX8797 Only)

The OVP circuit is designed to protect the CPU against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The MAX8796/MAX8797 continuously monitor the output for an overvoltage fault. The controller detects an OVP fault if the output voltage exceeds the set VID DAC voltage by more than 300mV, subject to a minimum OVP threshold of 0.8V. During pulse-skipping operation (DPRSLPVR = high), the controller initially sets the OVP threshold to a fixed transitional OVP threshold (1.8V for IMVP-6 or 1.55V for GMCH), which is equivalent to 300mV above the maximum VID code allowed. Once the output is in regulation (the first on-time is triggered) and the PWRGD blanking time expires, the controller tightens the OVP threshold, tracking the VID target by 300mV. During soft-start and soft-shutdown, the controller also uses the fixed transitional OVP threshold.

When the OVP circuit detects an overvoltage fault, the MAX8796/MAX8797 immediately force DL high, pull DH low. This action turns on the synchronous-rectifier MOSFETs with 100% duty and, in turn, rapidly discharges the output filter capacitor and forces the output low. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse will blow. Toggle $\overline{SHDN}$ or cycle the $V_{CC}$ power supply below 0.5V to clear the fault latch and reactivate the controller.

OVP protection can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

#### Output Undervoltage (UVP) Protection

The output UVP function limits the power loss by disabling the regulator if the MAX8796/MAX8797/MAX17401 output voltage drops 400mV below the target voltage; the controller activates the shutdown sequence and sets the fault latch. Once the controller ramps down to zero, it forces DL and DH low. Toggle $\overline{SHDN}$ or cycle the $V_{CC}$ power supply below 0.5V to clear the fault latch and reactivate the controller.

UVP protection can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

#### Thermal Fault Protection

The MAX8796/MAX8797/MAX17401 feature a thermal-fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor sets the fault latch, forces DL low, and pulls DH low. Toggle $\overline{SHDN}$ or cycle the $V_{CC}$ power supply below 0.5V to clear the fault latch and reactivate the controller after the junction temperature cools by 15°C. Thermal shutdown can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

#### No-Fault Test Mode

The latched fault-protection features can complicate the process of debugging prototype breadboards since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a “no-fault” test mode is provided to disable the fault protection—OVP, UVP, thermal shutdown, and TON open-circuit fault protection. The “no-fault” test mode also disables the BST switch, although the switch’s body diode provides sufficient power for the high-side driver to function properly. Additionally, the test mode clears the fault latch if it has been set. The no-fault test mode is entered by forcing 11V to 13V on $\overline{SHDN}$.

### MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large $V_{IN}$ - $V_{OUT}$ differential exists. The high-side gate drivers (DH) source and sink 2.2A, and the low-side gate drivers (DL) source 2.7A and sink 8A. This ensures robust gate drive for high-current applications. The DH high-side MOSFET driver is powered by an internal charge-pump boost switch at BST, while the DL synchronous-rectifier driver is powered directly by the 5V bias supply ($V_{DD}$).

Adaptive dead-time circuits monitor the DL and DH drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency.

There must be a low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX8796/MAX8797/MAX17401 interprets the MOSFET gates as “off” while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The internal pulldown transistor that drives DL low is robust, with a 0.25Ω (typ) on-resistance. This helps prevent DL from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX) quickly switches from ground to $V_{IN}$. Applications with high input voltages and long inductive driver traces must guarantee rising LX edges do not pull up the low-side MOSFET's gate, causing shoot-through currents. The capacitive coupling between LX and DL created by the MOSFET's gate-to-drain capacitance ($C_{RSS}$), gate-to-source capacitance ($C_{ISS}$ - $C_{RSS}$), and additional board parasitics should not exceed the following minimum threshold:

$$V_{GS(TH)} < V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Typically, adding a 4700pF between DL and power ground ($C_{NL}$ in Figure 13), close to the low-side MOSFETs, greatly reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays.

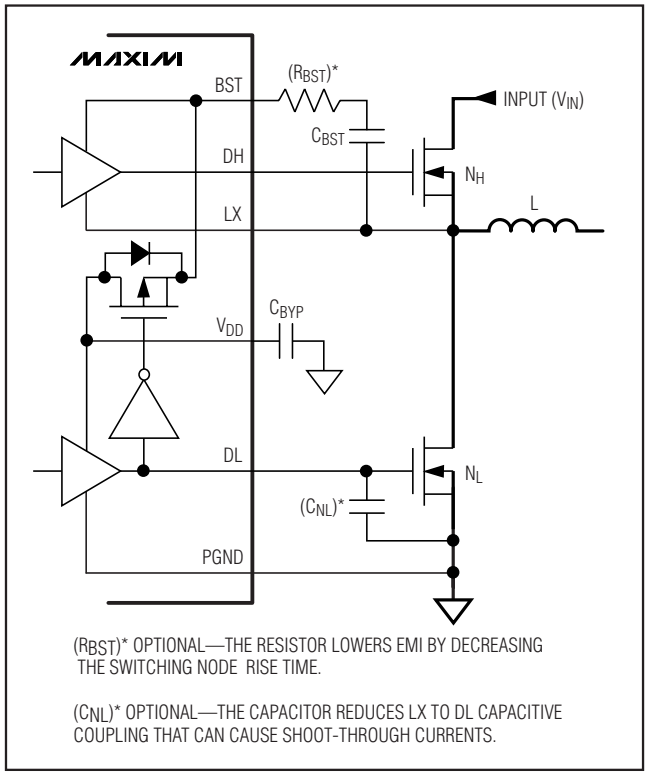



*Figure 13. Gate-Drive Circuit*

Alternatively, shoot-through currents can be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 5Ω in series with BST slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time ($R_{BST}$ in Figure 13). Slowing down the high-side MOSFET also reduces the LX node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

## Quick-PWM Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following five factors dictate the rest of the design:

- **Input voltage range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum load current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current ($I_{LOAD}$) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.
- **Load line (voltage positioning):** The load line (output voltage vs. load slope) dynamically lowers the output voltage in response to the load current, reducing the output capacitance requirement and the processor's power dissipation. The Intel specification clearly defines the load-line requirement in the power-supply specifications for each processor family.

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- **Switching frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage due to MOSFET switching losses that are proportional to frequency and $V_{IN}^2$. The optimum frequency is also a moving target due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor operating point:** This choice provides trade-offs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

### Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = \left(\frac{V_{IN} - V_{OUT}}{f_{SW} I_{LOAD(MAX)} LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Molded cores are often the best choice, although powdered iron and ferrite cores are inexpensive and can work well at 300kHz. The core must be large enough not to saturate at the peak inductor current ($I_{PEAK}$):

$$I_{PEAK} = I_{LOAD(MAX)}\left(1 + \frac{LIR}{2}\right)$$

### Transient Response

The inductor ripple current impacts transient-response performance, especially at low $V_{IN}$ - $V_{OUT}$ differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time. The worst-case output sag voltage can be determined by:

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})^2\left[\left(\frac{V_{OUT} t_{SW}}{V_{IN}}\right) + t_{OFF(MIN)}\right]}{2C_{OUT}V_{OUT}\left[\left(\frac{(V_{IN} - V_{OUT})t_{SW}}{V_{IN}}\right) - t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics* table).

The amount of overshoot due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2C_{OUT}V_{OUT}}$$

### Current-Limit and Slew-Rate Control (TIME and ILIM)

TIME and ILIM are used to control the slew rate and current limit. TIME regulates to a fixed 2.0V. The MAX8796/MAX8797/MAX17401 use the TIME source current to set the slew rate ($dV_{TARGET}/dt$). The higher the source current, the faster the output-voltage slew rate:

$$dV_{TARGET}/dt = 12.5mV/\mu s \left(\frac{71.5k\Omega}{R_{TIME}}\right)$$

where $R_{TIME}$ is the sum of resistance values between TIME and ground.

The ILIM voltage determines the valley current-sense threshold. When ILIM = $V_{CC}$, the controller uses the preset current-limit threshold—22.5mV for IMVP-6 designs (MAX8796/MAX17401: V3P3 = 3.3V) or 17.5mV for GMCH designs (MAX8797 or MAX8796/MAX17401: V3P3 = GND). In an adjustable design, ILIM is connected to a resistive voltage-divider connected between TIME and ground. The differential voltage between TIME and ILIM sets the current-limit threshold ($V_{LIMIT}$), so the valley current-sense threshold is:

$$V_{LIMIT} = \frac{V_{TIME} - V_{ILIM}}{10}$$

where the $V_{LIMIT}$ tolerances are defined in the *Electrical Characteristics* table.

This allows design flexibility since the DCR sense circuit or sense resistor does not have to be adjusted to meet the current limit as long as the current-sense voltage never exceeds 50mV. Keeping $V_{LIMIT}$ between 20mV to 40mV leaves room for future current-limit adjustment.

The minimum current-limit threshold must be high enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current; therefore:

$$I_{VALLEY} > I_{LOAD(MAX)} \left(1 - \frac{LIR}{2}\right)$$

where:

$$I_{VALLEY} = \frac{V_{LIMIT}}{R_{SENSE}} \quad \frac{V_{LIMIT}}{DCR \times \frac{R_{CSP-CSN}}{R_{LX-CSN}}}$$

where $R_{SENSE}$ is the sensing resistor and $R_{CSP-CSN}/R_{LX-CSN}$ is the ratio of resistor-divider with DCR-sensing approach.

### Voltage Positioning and Loop Compensation

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the output capacitance and processor's power dissipation requirements. The controller uses a transconductance amplifier to set the transient and DC output voltage droop (Figure 3) as a function of the load. This adjustability allows flexibility in the selected current-sense resistor value or inductor DCR, and allows smaller current-sense resistance to be used, reducing the overall power dissipated.

#### Steady-State Voltage Positioning

Connect a resistor ($R_{FB}$) between FB and $V_{OUT}$ to set the DC steady-state droop (load line) based on the required voltage-positioning slope ($R_{DROOP}$):

$$R_{FB} = \frac{R_{DROOP}}{R_{SENSE} \, G_{m(FB)}}$$

where the effective current-sense resistance ($R_{SENSE}$) depends on the current-sense method (see the *Current Sense* section), and the voltage-positioning amplifier's transconductance ($G_{m(FB)}$) is typically 600µS as defined in the *Electrical Characteristics* table. When the inductors' DCR is used as the current-sense element ($R_{SENSE} = R_{DCR}$), the current-sense design should include a thermistor to minimize the temperature dependence of the voltage-positioning slope as shown in Figure 1.

#### Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

In CPU $V_{CORE}$ converters and other applications where the output is subject to large-load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$(R_{ESR} + R_{PCB}) \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. The maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \left[\frac{V_{IN} f_{SW} L}{(V_{IN} - V_{OUT}) V_{OUT}}\right] V_{RIPPLE}$$

where $f_{SW}$ is the switching frequency. The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of polymer types).

When using low-capacity ceramic filter capacitors, capacitor size is usually determined by the capacity needed to prevent $V_{SAG}$ and $V_{SOAR}$ from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the $V_{SAG}$ and $V_{SOAR}$ equations in the *Transient Response* section).

#### Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi R_{EFF} C_{OUT}}$$

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and:

$$R_{EFF} = R_{ESR} + R_{DROOP} + R_{PCB}$$

where $C_{OUT}$ is the total output capacitance, $R_{ESR}$ is the total ESR, $R_{SENSE}$ is the current-sense resistance ($R_{CM} = R_{CS}$), $R_{DROOP}$ is the voltage-positioning slope, and $R_{PCB}$ is the parasitic board resistance between the output capacitors and sense resistors.

For a standard 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum, Sanyo POSCAP, and Panasonic SP capacitors in widespread use at the time of publication have typical ESR zero frequencies below 50kHz. In the standard GMCH application circuit, the ESR needed to support a 10mV$_{P-P}$ ripple is 10mV/(10A x 0.3) = 3.3mΩ. Two 330µF/2.5V Panasonic SP (type SX) capacitors in parallel provide 3.0mΩ (max) ESR. With a 5mΩ droop and 0.5mΩ PCB resistance, the typical combined ESR results in a zero at 28kHz.

Ceramic capacitors have a high-ESR zero frequency, but applications with significant voltage positioning can take advantage of their size and low ESR. Do not put high-value ceramic capacitors directly across the output without verifying that the circuit contains enough voltage positioning and series PCB resistance to ensure stability. When only using ceramic output capacitors, output overshoot ($V_{SOAR}$) typically determines the minimum output capacitance requirement. Their relatively low capacitance value can cause output overshoot when stepping from full-load to no-load conditions, unless a small inductor value is used (high switching frequency) to minimize the energy transferred from inductor to capacitor during load-step recovery.

Unstable operation manifests itself in two related but distinctly different ways: double pulsing and feedback loop instability. Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

### Input Capacitor Selection

The input capacitor must meet the ripple current requirement ($I_{RMS}$) imposed by the switching currents. The $I_{RMS}$ requirements can be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD}}{V_{IN}}\right)\sqrt{V_{OUT}(V_{IN} - V_{OUT})}$$

The worst-case RMS current requirement occurs when operating with $V_{IN} = 2 \times V_{OUT}$. At this point, the above equation simplifies to $I_{RMS} = 0.5 \times I_{LOAD}$.

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. If the Quick-PWM controller is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

### Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET ($N_H$) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both of these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of $N_H$ (reducing $R_{DS(ON)}$ but with higher $C_{GATE}$). Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of $N_H$ (increasing $R_{DS(ON)}$ to lower $C_{GATE}$). If $V_{IN}$ does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin SOs, DPAK, or $D^2PAK$), and is reasonably priced. Make sure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur (see the *MOSFET Gate Drivers* section).

### MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET ($N_H$), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$P_{D(NH\ resistive)} = \left(\frac{V_{OUT}}{V_{IN}}\right) I_{LOAD}^2 R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power dissipation often limits how small the MOSFET can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFET ($N_H$) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on $N_H$:

$$P_{D(NH Switching)} = V_{IN(MAX)} I_{LOAD} f_{SW} \left(\frac{Q_{G(SW)}}{I_{GATE}}\right) + \frac{C_{OSS} V_{IN}^2 f_{SW}}{2}$$

where $C_{OSS}$ is the $N_H$ MOSFET's output capacitance, $Q_{G(SW)}$ is the charge needed to turn on the $N_H$ MOSFET, and $I_{GATE}$ is the peak gate-drive source/sink current (2.2A typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the $C \times V_{IN}^2 \times f_{SW}$ switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET ($N_L$), the worst-case power dissipation always occurs at maximum input voltage:

$$P_{D(NL\ resistive)} = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right] I_{LOAD}^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$, but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, you can "over design" the circuit to tolerate:

$$I_{LOAD} = \left(I_{VALLEY(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}\right) = I_{VALLEY(MAX)}$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good-size heatsink to handle the overload power dissipation.

Choose a Schottky diode ($D_L$) with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time. Select a diode that can handle the load current during the dead times. This diode is optional and can be removed if efficiency is not critical.

### Boost Capacitors

The boost capacitors ($C_{BST}$) must be selected large enough to handle the gate-charging requirements of the high-side MOSFETs. Typically, 0.1µF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and $Q_{GATE}$ is the gate charge specified in the MOSFET's data sheet. For example, assume (2) IRF7811W n-channel MOSFETs are used on the high side. According to the manufacturer's data sheet, a single IRF7811W has a maximum gate charge of 24nC ($V_{GS}$ = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{2 \times 4nC}{200mV} = 0.24\mu F$$

Selecting the closest standard value, this example requires a 0.22µF ceramic capacitor.

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## Applications Information

### PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board with their ground terminals flush against one another. Follow the MAX8796 Evaluation Kit layout and use the following guidelines for good PCB layout:

- High-current path/components: Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- MOSFET drivers: Keep the high-current, gate-driver traces (DL, DH, LX, and BST) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.
- Analog control signals: Connect all analog grounds to a separate solid copper plane, which connects to the GND pin of the Quick-PWM controller as shown in Figures 1, 2, and 14. This includes the $V_{CC}$ bypass capacitor, remote-sense bypass capacitors, and the compensation (CCV) components.
- CSP and CSN connections for current limiting and voltage positioning must be made using Kelvin-sense connections to guarantee the current-sense accuracy.
- Route high-speed switching nodes (LX, DH, BST, and DL) away from sensitive analog areas (FB, CSP, CSN, CCV, etc.).

### Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, $C_{IN}$, $C_{OUT}$, and D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET. The DL gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC).
3) Group the gate-drive components (BST capacitor, $V_{DD}$ bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in the standard application circuits. This diagram can be viewed as having three separate ground planes: input/output system ground, where all the high-power components go; the power ground plane, where the PGND pin and $V_{DD}$ bypass capacitor go; and the controller's analog ground plane where sensitive analog components, the analog GND pin, and $V_{CC}$ bypass capacitor go. The analog GND plane must meet the PGND plane only at a single point directly beneath the controller. This star ground point (where the power and analog grounds are connected) should connect to the high-power system ground with a low-impedance connection (short trace or multiple vias) from PGND to the source of the low-side MOSFET.
5) Connect the output power planes ($V_{CORE}$ and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

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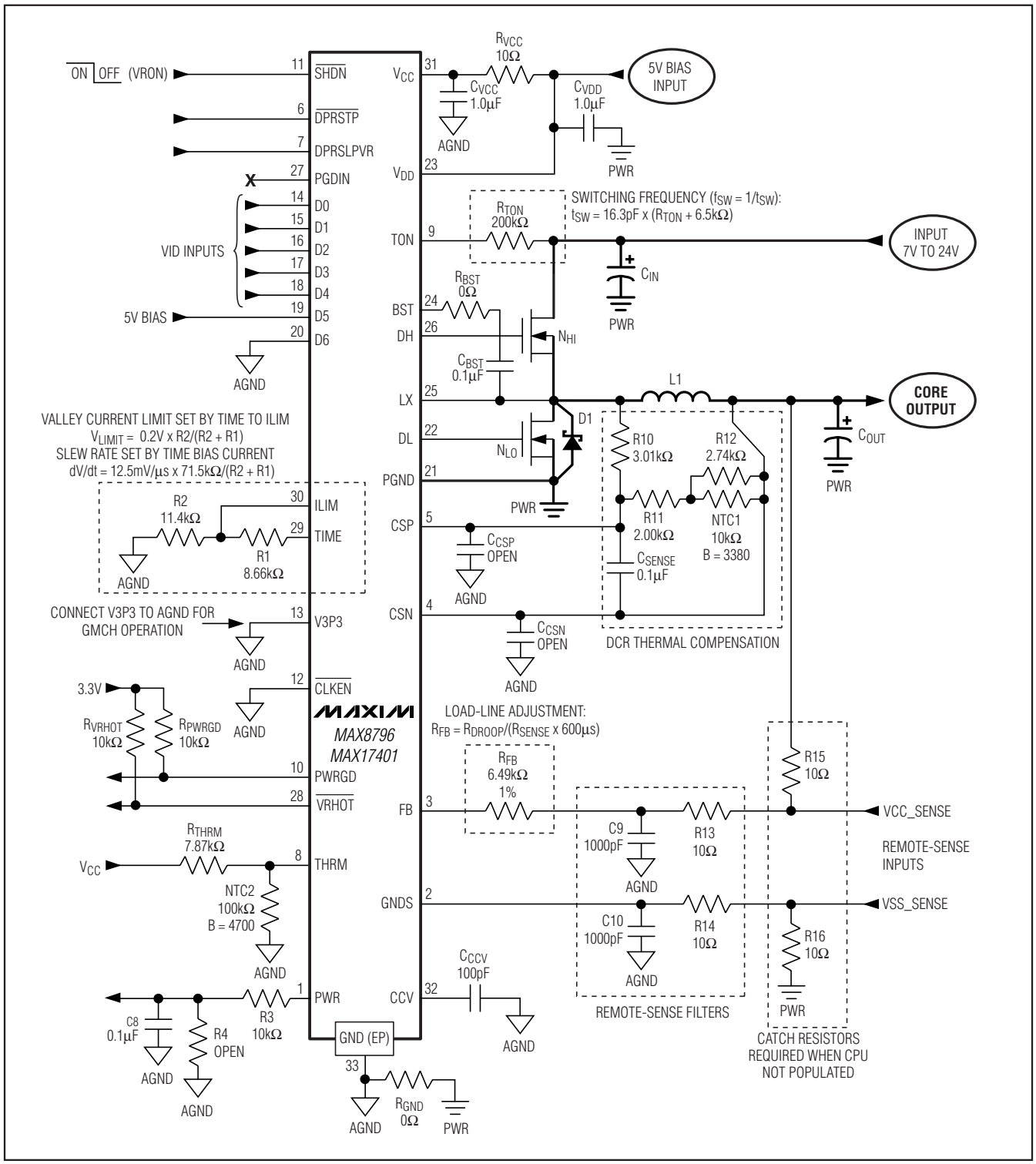


*Figure 14. MAX8796/MAX17401 GMCH Standard Application Circuit*

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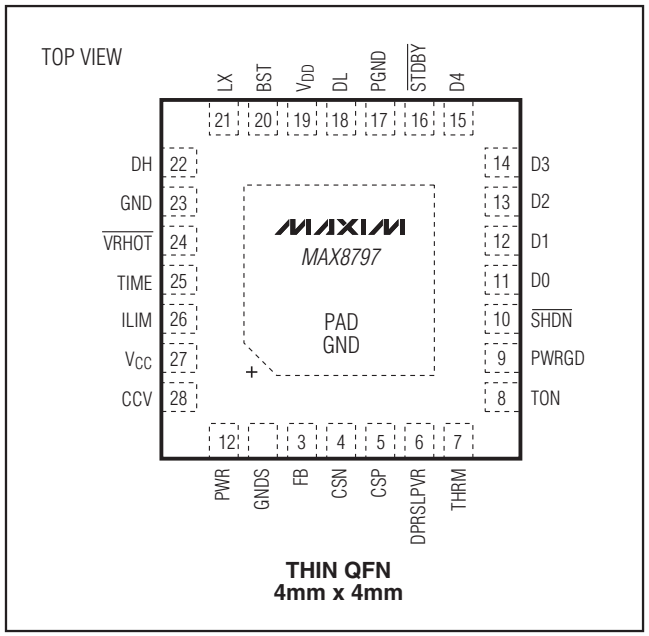
## Pin Configurations (continued)




**THIN QFN**
**4mm x 4mm**

## Chip Information

TRANSISTOR COUNT: 10,119

PROCESS: BiCMOS

## Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 32 TQFN | T3255-3 | **21-0140** |
| 28 TQFN | T2844-1 | **21-0139** |

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## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 11/07 | Initial release | — |
| 1 | 8/08 | Added MAX17401 | 47 |